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(57) Abstract :
The current invention is meant for realizing an AI Enabled method for Parasitic R & C estimation in progressive stacked SRAM circuits. In the process of IC design, the current invention provides methodology for identifying parasitic components of interconnect. In other words, it provides machine learning based approach to analyse data associated with circuits and discover parasitic RCs of interconnect lines. With multivariate Linear Regression (LR), the invention analyses dependent and independent variables to arrive at accurate predictions. Issues with interconnect lines are in the form of thickness, as the number of layers increases the interconnect layer thickness increases, which leads to use of higher dielectric layer with high permittivity. This causes the inter wire capacitance to rise. Such issues are addressed in the underlying methodology using ML algorithms as a novel approach for estimating the parasitic R, C considering progressive stacked SRAMs i.e. from 6T to 10T. The current invention is useful for different stakeholders like real world businesses, organizations, enterprises that have businesses across the globe and governments.

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