Patent Search

Invention Title	CARBON NANO-TUBE FIELD EFFECT TRANSISTOR BASED MEMORY DEVICE
Publication Number	24/2023
Publication Date	16/06/2023
Publication Type	INA
Application Number	202341020130
Application Filing Date	22/03/2023
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	ELECTRONICS
Classification (IPC)	B82Y 100000, G06F 303670, H01L 296600, H01L 510000, H01L 510500

Inventor

Name	Address	Country	Nationality
M.Parvathi	BVRIT HYDERABAD College of Engineering for Women, 8-5/4, Rajivgandhi Nagar, Bachupally, Hyderabad, Telangana – 500090, India	India	India

Applicant

Name	Address	Country	Nationality
BVRIT HYDERABAD College of Engineering for Women	8-5/4, Rajivgandhi Nagar, Bachupally, Hyderabad, Telangana – 500090, India	India	India

Abstract:

Disclosed is a memory device (100) including a first inverter (102), and a second inverter (104). The first inverter (102) includes a first p- type transistor (106) and a first n-type transistor (110) connected in series. The second inverter (104) cross-coupled to the first inverter (102), and includes a second p-type transistor (108) and a second n-type transistor (112) connected in series. The memory device (100) further includes a third n-type transistor (114) connected to a first input node (Q), and a fourth n-type transistor (116) connected to a second input node (Q'). At least one of the first and second p-transistors (106-108), and the first through fourth n-transistors (110-116), are implemented using carbon nano-tube field effect transistor (CNTFET).

Complete Specification

Description:TECHNICAL FIELD
The present disclosure relates to the technical field of embedded system design. More particularly, the present disclosure relates to a carbon nano-tube field effect transistor (CNTFET) based memory device.
BACKGROUND
Static Random-Access Memory (SRAM may be a critical component in embedded systems. The use of SRAMs in embedded systems is growing rapidly with the recent technological advancements. However, the embedded SRAMs are more prone to process and parametric variations under very deep sub-micron technologies (i.e., below 45 nano-metre (nm) technologies).
The SRAM must be capable of determining an accurate power dissipation in the embedded system (or a chip. it is employed into. As the process of scaling goes beyond 90nm technology, the contribution of leakage power to the total power dissipation increases randomly. The state of art SRAMs assume the temperature variation in the entire chip is considered to be constant, thus do not provide an accurate information of the contribution of the leakage power in the total power dissipation, which impacts the stability and performance of the embedded system.
Thus, a memory device that can increase the parametric yield by determining the power dissipation accurately, and understand the unknown gap between design and silicon results due to process variations, is an ongoing effort and demands a need for improvised technical solution that overcomes the aforementioned problems.
SUMMARY
In an aspect of the present disclosure, a memory device includes a first inverter cross coupled to a second inverter. The first inverter includes a first p- type transistor and a

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