Personal Information

Name	Dr. T Thammi Reddy
Years of Experience	Teaching: 17 years Industry: 07 years Research: NIL
Email Id (College Mail ID)	thammireddy@bvrithyderabad.edu.in
Areas of Specialization/Interest	VLSI, Embedded Systems, Processor Architectures

Educational Qualifications

Doctoral Degree	Ph.D.	JNTUH, Hyderabad, TS (VLSI)
PG Degree	M.Tech.	Microelectronics, IIT-BHU, Varanasi, UP.
UG Degree	B.Tech.	ECE, Sri Krishnadevaraya University (SKU), Anantapuramu, AP.

Papers Published

International Journal Publications

1. **T. Thammi Reddy**; B.K. Madhavi; K. Lal Kishore, "Area Efficient SDR Receiver with and without dynamic partial reconfiguration," in Special Issue on "Soft Computing Approaches and Intelligent Systems" of the *International Journal of Intelligent Systems Technologies and Applications (IJISTA)* by INDERSCIENCE. (SCOPUS), ACM Digital Library, Volume 17, Nos 1/2, 2018. pp 176-194; ISSN online: 1740-8873, ISSN print: 1740-8865.
2. Chaitanya, M; **T. Thammi Reddy**; Rajeswari, C; Haritha, G, "Irrigation Automation using IoT," Journal of Test, Engineering and Management ISSN: 0193 - 4120, Volume 82, Jan-Feb (2020), PP. 12377-12383
3. R. Mounika and **T. Thammi Reddy**," Design of Low power and high-performance Full Subtractor circuits by using 5T based XOR and XNOR combo gate", *Test Engineering and Management, The Mattingly Publishing Co. Inc*, Volume 83, (SCOPUS), ISSN: 0193-4120, PP: 6639-6645, May-June (2020)
4. Reddy, I. Sumanth Kumar; **T. Thammi Reddy**, "Analysis of DDS using Reversible Logic and CORDIC algorithm", International Journal of Recent Technology and Engineering (IJRTE), (SCOPUS). ISSN:2277-3878, Vol11, 03-Special Issue (2019)
5. Raghunandan, Avula; **T. Thammi Reddy**, "Implementation of Efficient FIR Filter Using Coefficient Synthesis Genetic Algorithm" Journal of Advanced Research in Dynamical and Control Systems (JARDCS), Vol. 10, Special Issue 03-, (SCOPUS), PP: 1326-1333, ISSN 1943-023X, (2018)
6. M. Mounika, and **T. Thammi Reddy**," International Journal of Engineering Science and Generic Research, Implementation of SHA-2(256) & SHA-3(512) Algorithms for Information Security.", *International Journal of Engineering Science and Generic Research (IJESAR),* Volume 2, Issue 5, (2016), ISSN: 2456-043X
7. Mehjabeen, A., and **T. Thammi Reddy**," Implementation of Reusable DCT Architectures with Reversible Adders." *International Journal & Magazine of Engineering, Technology, Management and Research (IJMETMR), Yuva Engineers Publications*, Volume 3, Issue 10, (2016). ISSN: 2348-4845
8. Saipriya, G., and **T. Thammi Reddy**. "VHDL Implementation of Audio Processing Using Adaptive Filter." *International Journal of Science, Engineering and Technology Research (IJSETR),* (2015)
9. Bhargavi, C., and **T. Thammi Reddy**. "Designing of High-Performance Floating-Point Processing Element for Reconfigurable Systems." *Journal of Innovation in Electronics and Communication Engineering* 5.1 PP: 34-42. (2015)
10. Madhavi, S., And **T. Thammi Reddy**. "Implementation of High-Speed MDC FFT/IFFT Processor for MIMO-OFDM Systems." *International Journal of Science, Engineering and Technology Research* (*IJSETR*) (2015).
11. Tanveer, D., and **T. Thammi Reddy**. "A 2-D DCTT Computation Based on Bivariate Algebraic Integer using Single Channel Architecture." *International Journal of Emerging Trends in Engineering and Development*, (2014)

12. Kamalesh, G., and **T. Thammi Reddy**. "FPGA implementation of high-speed PI like Fuzzy Control System for Industrial Automation Applications", *International Journal of Modern Engineering Research*, PP: 1447-1453, 3.3, (2013)
13. Vijaya Kumar. B., **T. Thammi Reddy**, "FPGA Implementation of High-Speed AES Algorithm for Improving the System Computing Speed", *International Journal of Computer Trends and Technology (IJCTT)*, Seventh Sense Research Group, Volume 4, Issue 9, PP: 2981-2985, ISSN 2231-2803, (2013)

International Conference Publications

1. **T. Thammi Reddy**; B.K. Madhavi; K. Lal Kishore, "Area Efficient SDR Receiver with Dynamic Partial Reconfiguration," *Inventive Research in Engineering and Technology (ICIRET)*, 2017 Inventive Research Organization (IRO) International Conference on, Bangkok, Thailand January 2017, pp 244-257; ISBN: 978-81-932480-1-0.
2. **T. Thammi Reddy**; B.K. Madhavi; K. Lal Kishore, "Area Efficient Implementation of FSK Receiver on Xilinx Zynq FPGA," in *Inventive Computation Technologies (ICICT), 2016 IEEE International Conference on*, vol. no.1 pp.0184-0190, 26-27 August 2016, Coimbatore, India. Print ISBN: 978-1-5090-12
3. **T. Thammi Reddy**; B.K. Madhavi; K. Lal Kishore, "Improved block-based processing with dual partial reconfiguration memory approach," in *Communications and Signal Processing (ICCSP), 2015 IEEE International Conference on*, vol., no., pp.0327-0331, 2-4 April 2015, Melmaruvathur, India.; Print ISBN: 978-1-4799-8080-2;
4. **T. Thammi Reddy**; T. Janardhan Reddy; B.K. Madhavi, "Reconfigurable Higher-Order IIR Filter Implementation on Zynq Platform with Low Resource Utilization" *Journal of Advanced Research in Dynamical and Control Systems (JARDCS)* ISSN: 1794-023X, (SCOPUS)
5. **T. Thammi Reddy**; Reddy, T. Janardhan; Madhavi, B. K, "Zynq-7000 AP SoC Implementation of Configurable Folded IIR Filter Design", *Trends in Engineering, Management, Pharmacy & Sciences (ICTEMPS) 2018 International Conference on*, 21st April 2018, Hyderabad, INDIA.

National Journal Publications: -

National Conference Publications

1. **T. Thammi Reddy**; B.K. Madhavi; K. Lal Kishore, "Reconfigurable Computing: A Taxonomical Survey," in Proceedings of *National Conference on Computing Communication & Instrumentation (NCCCI'12)*, Dec 2012, Hyderabad, India. Print ISBN: 978-81-923724-1-9

FDPs/Workshops Conducted:

1. Organized National FDP, "Recent Developments in VLSI Design and Its Research Trends" as convener from 30th Aug 2021 to 3rd Sep 2021 in GPREC Kurnool AP as convener.
2. Organized as moderator for a panel discussion on "How Can Our Engineering Graduate Be Industry Ready" at GPREC, Kurnool on 2nd Aug 2020.
3. Organized as a resource person for a webinar on "Formal Verification: Significance in VLSI Design Flow & SystemVerilog Assertions (SVA)" at GPREC, Kurnool on 12th June 2020.
4. Organized as a resource person for a 1-day da National level Workshop on VLSI Fabrication Principles and FPGA Design Flow (VFPFD-19) at GPREC, Kurnool on 17th June 2019.

MOOCs Completed

1. Hardware Modeling Using Verilog for 8 weeks during Aug-Oct 18 (NPTEL)
2. Introduction to Electronics for 4 weeks during May 2020 (Coursera)
3. Introduction to FPGA Design for Embedded Systems for 4-weeks during May 2020 (Coursera)
4. Embedded Hardware and Operating Systems for 4-weeks during May 2020 (Coursera)
5. Introduction to the Internet of Things and Embedded Systems for 4 weeks during May 2020 (Coursera)
6. How Computers Work for 4 weeks during May 2020 (Coursera)
7. Programming for Everybody (Getting Started with Python) for 4-weeks during May 2020 (Coursera)

FDPs and Workshops attended:

1. FDP on "Intellectual Property Rights" at GPREC, Kurnool, AP during 13 Jul- 17 July 2020
2. FDP on "IoT & Machine Learning" at GPREC, Kurnool, AP from 26 Jun-30 Jun 2020
3. Online "Partial Reconfigurable FPGA/SoC Xilinx Vivado" FDP by Apply Volt, Vijayawada, AP during 20-24 Jun 2020
4. FDP on "MOODLE LMS" by ATAL, IIITDM, Kurnool, AP during 21-22 May 2020
5. Online FDP on "VLSI Analog & Digital Design Perspective" by JNTUA Anantapur, AP during 16-17 May 2020
6. Online FDP on "Design, Implementation, and Verification" in VLSI by Sandeepani, Bengaluru during 27 Apr-1 May 2020
7. Online FDP on "ASIC Physical Design and Verification" by EXCEL VLSI, Bengaluru from 27 Apr-02 May 2020
8. Online FDP on "ASIC Synthesis and Static Timing Analysis" by EXCEL VLSI, Bengaluru during 20-25 Apr 2020

9. Tutorial on "IEEE VLSI Design" 2020 International Conf. by IEEE, Bengaluru during 4-8, Jan 2020
10. FDP on "Internet of Things" by ATAL, IIITDM Kurnool, AP during 15 Dec-19 Dec 2019
11. FDP on "Artificial Intelligence" by ATAL, IIITDM Kurnool, AP during 28 Nov-02 Dec 2019
12. FDP on "Designing with Zynq SoC and Its Applications" UIIC, JNTUH, Hyderabad during 16-18 October 2019
13. FDP on "DNA Of Mixed Signal IC design for portable Systems" by E&ICT, NIT Warangal, TS during 20-25 May 2019
14. FDP on "Outcome-Based Education (OBE)" by E&ICT, NIT Warangal & IIITDM-Kurnool, AP during 6-11 May 2019
15. FDP on "Adv Embedded. System Design on Zynq Ultra Scale+ using Vivado" by CoreEL Bengaluru & JNTUH, Hyderabad during 30 Jul-3 Aug 2018
16. FDP on "Programming Xilinx Zynq SoCs with MATLAB and Simulink" by MATHWORKS, Hyderabad during 26-27 July 2017
17. FDP on "Generating HDL Code from Simulink" by MATHWORKS, Hyderabad during 24-25 July 2017
18. FDP on "CMOS, Mixed Signal, Radio Frequency VLSI Design" by MHRD, IIT-KGP & GPREC, Kurnool, AP during 26 Dec-4 Jan 2017
19. FDP on "VLSI Design" by APSSDC & SRKIT-Vijayawada during 15-9 Nov 2016
20. Workshop on "SoC Physical Design using CADENCE" by GPREC, Kurnool, AP during 4-5 Mar 2016
21. FDP on "Instructional Excellence in Intelligent Systems", FICE, INTEL & GPREC, Kurnool, AP during 17-19 Apr 2014
22. Workshop on "Analog and Digital CMOS Design flow using Mentor Graphics EDA Tools" by Mentor Graphics & GPREC, Kurnool, AP during 28-29 Nov 2012
23. Tutorial 25th International Conf.: "VLSI Design" IEEE, Hyderabad Chapter 7-11 during Jan 2012
24. FDP on "Embedded System-ARM" by MGIT, Hyderabad during 2-4 Dec 2009
25. Workshop on "Low Power VLSI Design" by MIST, Hyderabad during 22-23 Mar 2007
26. Workshop on "Nano-Electronics" by CBIT, Hyderabad during 25-26 Nov 2006

Professional Memberships:

1. Member of IEEE since 2012 with Membership No.: 92013805

Any Other Achievements:

1. Supervised 20 M.Tech students with their major project work in the VLSI domain.
2. Gained experience working with inter-disciplinary and multi-cultural teams in Japan and the USA.
3. Contributed to curriculum development, as BoS member, for 6 years at GPREC, Kurnool, AP.