

ACADEMIC REGULATIONS (BH25)
COURSE STRUCTURE
AND
DETAILED SYLLABUS

VLSI Design

for

M.Tech. Two Year Degree Course

(Applicable for the batches admitted from 2025-26 onwards)



BVRIT HYDERABAD College of Engineering for Women

(UGC Autonomous Institution | Approved by AICTE | Affiliated to JNTUH)
(NAAC Accredited – A Grade | NBA Accredited B.Tech. (EEE, ECE and CSE))

Bachupally, Hyderabad -500 090

www.bvrithyderabad.edu.in

BVRIT HYDERABAD College of Engineering for Women

VISION

To emerge as the best among the institutes of technology and research in the country dedicated to the cause of promoting quality technical education.

MISSION

At BVRITH, we strive to

- Achieve academic excellence through innovative learning practices.
- Enhance intellectual ability and technical competency for a successful career.
- Encourage research and innovation.
- Nurture students towards holistic development with emphasis on leadership skills, life skills and human values.

CORE VALUES

1. Holistic Development
2. Excellence in Education
3. Women Empowerment
4. Integrity
5. Social Responsibility
6. Accountability and Transparency
7. Freedom of Expression

Department of Electronics and Communication Engineering

VISION

To emerge as a centre of academic and research excellence in Electronics and Communication Engineering and create globally competent women technocrats with a high degree of social consciousness in a holistic learning environment.

MISSION

M1: To provide quality education to the students with emphasis on training related to latest technologies as per industrial needs

M2: To impart research culture, professional ethics and moral values to the students by committed and competent faculty striving for excellence.

M3: To inculcate a perceptive alacrity in students to identify real life problems, formulate strategies and evolve into contextually effective solutions.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

After 3 to 6 years of graduation, students will be able to:

PEO-1: Excel in professional skills related to IC design, verification, and physical implementation to contribute effectively to the semiconductor industry.

PEO-2: Foster innovation by engaging in applied research, adopting emerging EDA tools and developing solution frameworks in VLSI applications.

PEO-3: Demonstrate professional ethics, human values, and interpersonal skills to work responsibly and effectively in diverse professional environments.

PROGRAM OUTCOMES (POs)

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: An ability to design and verify digital, analog and mixed-signal sub-systems using appropriate Electronic Design Automation tools and reconfigurable FPGA hardware.

PO5: An ability to optimize VLSI circuits and systems to meet the performance, power, area and reliability constraints.

PO6: An ability to integrate concepts from multi-disciplinary domains with VLSI design to develop efficient hardware–software solutions.



**Academic Regulations (BH25) for M.Tech (Regular / Full Time) Programme (CBCS)
(Effective for the students admitted from the Academic Year 2025-26 and onwards)**

Jawaharlal Nehru Technological University Hyderabad (JNTUH) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programmes, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

1.0 Post Graduate Degree Programme in Engineering & Technology (PGP in E & T)

BVRIT HYDERABAD College of Engineering for Women (Autonomous) – BVRITHCEW (A) offers new regulations termed as BH25 for **Two** Year (**Four** Semesters) full time Master of Technology (M.Tech.) Degree Programme, under Choice Based Credit System (CBCS) with effect from the Academic Year 2025-26 onwards, in the following Branches of Engineering

S.No	Branch Code	Specialization
1	B0	Data Sciences
2	A5	VLSI Design
3	58	Computer Science and Engineering

2.0 Eligibility for Admissions

- 2.1** Admission to the M.Tech. Programme shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M.Tech. Programme
- 2.2** Admission to the post graduate programme shall be made on the basis of either the Merit rank or Percentile obtained by the qualified student in the GATE Examination / the merit rank obtained by the qualified student in an entrance test conducted by Telangana Government (PGE CET) for M.Tech. Programmes / an entrance test conducted by JNTUH / on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.
- 2.3** The medium of instructions for all PG Programmes will be in **ENGLISH** only.

3.0 M.Tech Programme Structure

- 3.1** The M.Tech. Programs of JNTUH are of Semester pattern, consisting of **Two** academic years, each academic year having **Two** Semesters (Odd and Even Semesters).
- 3.2** The two-year M. Tech. program consists of **68** credits and the student has to register for all **68** credits and earn all **68** credits for the award of M. Tech. degree
- 3.3** The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.
- 3.4** **UGC / AICTE** specified definitions / descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme

There shall be a minimum of 15 weeks of instruction, excluding the mid-term and semester-end exams. Around 15 instruction hours, 30 instruction hours and 45 hours of learning need to be followed per one credit of theory course, practical course and project / field-based learning respectively. In each semester, there shall be ‘Continuous Internal Evaluation (CIE)’ and ‘Semester End Examination (SEE)’ under Choice Based Credit System (CBCS). The curriculum /course structure suggested by AICTE is followed as a reference document.

3.4.2 Credit Courses

All courses are to be registered by the student in a semester to earn credits which shall be assigned to each course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour / week / semester for theory / lecture (L) Courses or Tutorials (T)
- One credit for two hours / week / semester for Laboratory / Practical (P) courses
- One credit is allocated for three hours per week in a semester for Project / Mini-Project session.

3.4.3 Course Classification

S.No	Broad Course Classification	Course Group / Category	Course Description
1	Core Courses (CoC)	PC – Professional Core	Includes courses related to the parent discipline/department/ branch of Engineering
		Dissertation	M.Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline / Department / Branch of Engineering
2	Elective Courses (EtE)	PE – Professional Electives	Includes elective courses related to the parent discipline / department / branch of Engineering
		OE – Open Electives	Elective courses which include inter-disciplinary courses or courses in an area outside the parent Discipline / department / branch of Engineering
3	Audit Courses	--	Non Credit Audit Courses

4.0 Course Registration

- 4.1 A Faculty Advisor or Counsellor shall be assigned to each specialization, who will advise on the Post Graduate Programme, its Course Structure and Curriculum, Choices / Options for Courses, based on her competence, progress, pre-requisites and interest

- 4.2 The Registration Requests for any current semester shall be completed in time
- 4.3 A Student can apply for Registration, only after obtaining the written approval from her Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department and the Student).
- 4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during Registration for the Course(s) under a given / specified Course Group / Category as listed in the Course Structure, only the first mentioned Course in that Category will be taken into consideration.
- 4.5 Course Options exercised through Registration are final and cannot be changed. Further, alternate choices will not be considered. However, if the Course that has already been listed for Registration by the University in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Course, if it is offered, or for another existing Course (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the first week from the commencement of Class-work for that Semester.

5.0 Attendance Requirements

Attendance is calculated separately for each course.

- 5.1 Attendance in all classes (Lectures / Laboratories) is compulsory. The minimum required attendance in each theory course (**also Audit Courses**) including the attendance of mid-term examination / Laboratory etc. is 75%. Two periods of attendance for each theory course shall be considered, if the student appears for the mid-term examination of that course. ***This attendance should also be included in the attendance uploaded every fortnight in the University Website. The attendance of Audit Courses should be uploaded separately to the University.*** A student shall not be permitted to appear for the Semester End Examinations (SEE), if her attendance is less than 75%.
- 5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if she ensures minimum of 75% of her attendance in Seminar presentation classes on Mini Project during that Semester.
- 5.3 **Condoning of shortage of attendance** up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each course (Theory / Lab / Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.
- 5.4 A prescribed fee per course shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student
- 5.5 Shortage of Attendance below 65% in any course shall in **no case be condoned**
- 5.6 A Student, whose shortage of attendance is not condoned in any course(s) (Theory / Lab / Mini Project with Seminar) in any Semester, is considered as 'Detained in that course(s), and is not eligible to write Semester End Examination (s) of such course (s), in

that Semester; and she has to seek re- registration for those course (s) in sub sequent Semesters, and attend the same as and when offered

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 a) A student shall put in a minimum required attendance in at least three theory courses (excluding Audit course) in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least three theory courses (excluding *Audit* course) in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in clause no. 5. The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks per course (theory / practical), based on Continuous Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course, if she secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
- A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing '**B**' Grade or above in a course.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all courses for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of '**B**' Grade or above in each course, and shall ***pass all the Audit Courses*** to complete the M.Tech. Programme successfully

Note:

(1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the courses offered and gets minimum B grade in all the courses.

(2) CGPA is calculated only when the candidate passes in all the courses offered in all the semesters

6.4 Letter Grades obtained in all those courses covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the consolidated grade memo.

- 6.5 When a student is detained due to shortage of attendance in any course(s) in any semester, shall not be permitted to write the Semester End Examinations. However, she is eligible for re-registration of such course(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch in to which she is re-registered, by paying the prescribed fees per course. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation in such course(s), and SGPA/CGPA calculations.
- 6.6 A student eligible to appear for the Semester End Examination in any course, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that course at the supplementary examination as and when conducted. In such cases, her Internal Marks assessed earlier for that course will be carried over, and added to the marks secured in the supplementary semester end examination, for the purpose of evaluating her performance in that course.
- 6.7 A Student who fails to earn **68** credits as per the specified course structure, and as indicated above, within **four** academic years from the date of commencement of first year first semester, shall forfeit her seat in M. Tech. programme and admission **shall stand cancelled**

7.0 Evaluation – Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated course- wise (irrespective of credits assigned) for a maximum of 100 marks.

- 7.1 The performance of a student in every course (including practical's and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation for theory courses shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid- Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction
- 7.2 In CIE, for theory courses, during a semester, there shall be two mid-term examinations. Each Mid-Term examination consists of two parts i) **Part – A** for 10 marks, ii) **Part – B** for 20 marks with a total duration of two hours as follows:
1. Mid-Term Examination for 30 marks:
 - a. Part-A: Objective / Quiz paper for 10 Marks.
 - b. Part-B: Descriptive Paper for 20 Marks

The objective / quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks. The descriptive paper shall contain 6 full questions out of which, the student has to answer 4 questions, each carrying 5 marks. The average of the two Mid Term Examinations shall be taken as the final marks for Mid Term Examination for 30 marks

The remaining 10 marks of Continuous Internal Assessment (out of 40) are distributed as:
 2. 5 Marks for Assignment.(Average of 2 Assignments each for 5 marks)
 3. Course Viva-Voce / PPT / Poster Presentation / Case Study on a topic in the concerned course for 5 marks

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus. Five (5) marks are allocated for assignments (as specified by the course teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment.

Course Viva-Voce / PPT / Poster Presentation / Case Study on a topic in the concerned course for five marks before II Mid-Term Examination

The Student, in each course, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned course, if the students cores $\geq$ 40% (16marks) of 40 Continuous Internal Examination (CIE) marks

In case, the student appears for Semester End Examination (SEE) of the concerned course but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), her performance in that course in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are explained in the next clause

- 7.3** The Semester End Examinations (SEE), for theory courses, will be conducted for 60 marks consisting of two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.
- Part-A is a compulsory question which consists of ten sub-questions with uniform coverage from all units carrying equal marks
 - Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these questions is from each unit and may contain sub-questions. For each question there will be an “either” “or” choice, which means that there will be two questions from each unit and the student should answer either of the two questions
 - The duration of Semester End Examination is three hours.
- 7.4** For practical courses there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation
1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components / procedure, expected outcome) which shall be evaluated for 10 marks
 2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned
 3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks
 4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

In the Semester End Examination, held for three hours, total 60 marks are divided and allocated as shown below

1. 10 Marks for Write Up
2. 15 Marks for Experiment / Program
3. 15 for Evaluation of Results
4. 10 Marks for Presentation on another experiment / program in the same laboratory course and
5. 10 Marks for Viva-voce on concerned laboratory course

The Student, in each course ,shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned course, if the student scores $\geq 40\%$ (16marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned course but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks),her performance in that course in SEE shall stand cancelled inspite of appearing the SEE.

- 7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to the Director of University Examinations within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College concerned but within the cluster. No external examiner should be appointed from any other College in the same cluster/any other cluster which is run by the same Management.
- 7.6 There shall be Mini Project with Seminar during I year II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during the seminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluated by the DAC for another 50 marks before the semester end examinations. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If she fails to obtain the minimum marks, she has to reappear for the same as and when scheduled.
- 7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee
- 7.8 The M.Tech. Dissertation shall be prepared in the structure prescribed by the University, adhering to the style files and formatting guidelines. To facilitate this process, each institution will organize a brief orientation session for the entire class/section at the beginning of the final semester, guiding the students on the required structure and formatting of the dissertation

- 7.9 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme
- 7.10 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work after satisfying the attendance requirement in all the courses, both theory and laboratory.
- 7.11 After satisfying the previous clause, a candidate must present in **Dissertation Work Review-I**, in consultation with her Dissertation Supervisor, the title, objective and plan of action of her Dissertation work to the Dissertation Review Committee (DRC) for approval **within four weeks** from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.
- 7.12 If a candidate wishes to change supervisor or topic of the Dissertation, she can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change of her initial plans of Dissertation proposal. If yes, her date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
- 7.13 A candidate shall submit her Dissertation progress report in two stages at least with a gap of **three** Months between them
- 7.14 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC **not earlier than 40 weeks** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC
- 7.15 **The Dissertation Work Review - II** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If she fails to obtain the minimum required marks, she has to reappear for Dissertation Work Review - II as and when conducted.
- 7.16 The Dissertation Work Review - III in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review-III. If she fails to obtain the required minimum marks, she has to reappear for Dissertation Work Review- III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.

- 7.17** Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review-III (Phase I). These students shall reappear for Dissertation Work Review- III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review-III (Phase II) shall reappear for Dissertation Work Review-III in the next academic year only at the time of Dissertation Work Review - II (Phase I).
- 7.18** After approval from the DRC, a soft copy of the thesis should be submitted for Anti-Plagiarism check and the plagiarism report should be submitted to the University and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index is more than the required percentage, the student is advised to revise the thesis and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to **TWO**. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled
- 7.19** Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College / School / Institute
- 7.20** The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College / School / Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.
- 7.21** If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission
- 7.22** If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.
- 7.23** If she fails to fulfill the requirements as specified in the above clause, he will reappear for the Dissertation Viva-Voce examination **only after three months**. In the reappeared examination also, if she fails to fulfill the requirements, she will not be eligible for award of the degree, unless she is asked to revise and resubmit her Dissertation Work by the board within a specified time period
- 7.24** The Dissertation Viva-Voce External examination marks must be submitted to the University on the same day of the examination

- 7.25 For Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the course. These marks should also be uploaded along with the internal marks of other courses
- 7.26 No marks or letter grades shall be allotted for Audit Courses. Only Pass / Fail shall be indicated in Grade Card.

8.0 Re-Admission / Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M.Tech. degree programme due to any reason what so ever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which she gets readmitted, with prior permission from the authorities concerned

- 8.2 If a student is detained in a course (s) due to shortage of attendance in any semester, she may be permitted to **re-register** for the same course(s) or the student may register in an equivalent course, If the same course is not available, as suggested by the Board of Studies of that department, in the subsequent semester(s), with the academic regulations of the batch into which she seeks re-registration, with prior permission from the authorities concerned.
- 8.3 A candidate shall be given chance to re-register any number of courses, if the candidate failed in these courses due to securing less than 40% marks in CIE. A candidate must re-register for failed courses within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, her Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the current semester only will be accepted, if she secures pass grade.

9.0 Examinations and Assessment – The Grading System

- 9.1 Grades will be awarded to indicate the performance of each student in each Theory Course, or Lab / Practical's, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together), and a corresponding Letter Grade shall be given.
- 9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed

% of Marks Secured in a Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
90% and above ($\geq 90\%$, ≤ 100)	O (Outstanding)	10
Below 90% but not less than 80% ($\geq 80\%$, $< 90\%$)	A ⁺ (Excellent)	9
Below 80% but not less than 70% ($\geq 70\%$, $< 80\%$)	A (Very Good)	8
Below 70% but not less than 60% ($\geq 60\%$, $< 70\%$)	B ⁺ (Good)	7
Below 60% but not less than 50%	B (Above Average)	6

($\geq 50\%$, $< 60\%$)		
Below 50% ($< 50\%$)	F (Fail)	0
Absent	Ab	0

- 9.3** A student obtaining 'F' Grade in any Course is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, her Internal Marks (CIE Marks) in those courses will remain as obtained earlier.
- 9.4** If a student has not appeared for the examinations, 'Ab' Grade will be allocated to her for any course and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.
- 9.5** A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks
- 9.6** In general, a student shall not be permitted to repeat any Course (s) only for the sake of 'Grade Improvement' or 'SGPA / CGPA Improvement'
- 9.7** A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by her in that Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Course

Credit Points (CP)=Grade Point(GP) x Credits....For a Course

- 9.8** The student passes the Course only when she gets $GP \geq 6$ (B Grade or above).
- 9.9** The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points secured from all Courses registered in a Semester, by the total number of credits offered in that Semester. SGPA is rounded off to two decimal places. SGPA is thus computed as

$$SGPA = \left\{ \sum_{i=1}^N C_i G_i \right\} / \left\{ \sum_{i=1}^N C_i \right\} \dots \text{For each Semester}$$

where 'i' is the Course indicator index (taking into account all Courses in a Semester), 'N' is the no. of Courses offered in the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Course, and G_i represents the Grade Points corresponding to the Letter Grade awarded for that i^{th} Course

- 9.10** The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in all registered Courses in all Semesters, and the Total Number of Credits registered in all the Semesters. CGPA is rounded off to two decimal places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$CGPA = \left\{ \sum_{j=1}^M C_j G_j \right\} / \left\{ \sum_{j=1}^M C_j \right\}$$

9.10 (ie., up to and inclusive of S Semesters, $S \geq 2$),

where 'M' is the total no. of Courses (as specifically required and listed under the Course Structure of the parent Department) the Student has 'registered'. C_j is the no. of Credits allotted to the j^{th} Course, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Course. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects

Illustration of Calculation of SGPA

Course	Credits	Letter Grade	Grade Points	Credit Points
Course 1	4	A	8	$4 * 8 = 32$
Course 2	4	O	10	$4 * 10 = 40$
Course 3	4	B	6	$4 * 6 = 24$
Course 4	3	B	6	$3 * 6 = 18$
Course 5	3	A+	9	$3 * 9 = 27$
Course 6	3	B	6	$3 * 6 = 18$
	21			159
SGPA = $159 / 21 = 7.57$				

Illustration of Calculation of CGPA from SGPA

Course	Credits	SGPA	Credits * SGPA
Semester I	24	7	$24 * 7 = 168$
Semester II	24	6	$24 * 6 = 144$
Semester III	24	6.5	$24 * 6.5 = 156$
Semester IV	24	6	$24 * 6 = 144$
	96		612
CGPA = $612 / 96 = 6.37$			

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme, and secures the required number of **68** Credits (with CGPA ≥ 6.0), shall be declared to have 'qualified' for the award of the M.Tech. Degree in the chosen Branch of Engineering/Technology with the specialization that she was admitted into

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, she shall be placed in one of the following three classes based on the CGPA

Class Awarded	CGPA
First Class with Distinction	≥ 7.50
First Class	$6.50 \leq \text{CGPA} < 7.50$
Second Class	$6.00 \leq \text{CGPA} < 6.50$

A student with final CGPA (at the end of the **PGP**) < 6.00 shall not be eligible for the Award of Degree.

11.0 With holding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against her, the result and degree of the student will be withheld and she will not be allowed into the next semester

12.0 Conversion of CGPA in to equivalent Percentage of Marks

The following formula shall be used for the conversion of CGPA into equivalent marks, whenever it is necessary

$$\text{Percentage (\% of Marks)} = (\text{Final CGPA} - 0.5) \times 10$$

13.0 Mapping with the Sustainable Development Goals

All the courses specified in the course structure of every programme are mapped with the one or more sustainable development goals

14.0 General

14.1 Credit: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week

14.2 Credit Point: It is the product of grade point and number of credits for a course

14.3 The academic regulation should be read as a whole for the purpose of any interpretation

14.4 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final

14.5 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University

BVRIT HYDERABAD College of Engineering for Women

(UGC Autonomous Institution | Approved by AICTE | Affiliated to JNTUH)
(NAAC Accredited – A Grade | NBA Accredited B.Tech. (EEE, ECE and CSE))
Bachupally, Hyderabad -500 090

M.Tech. in VLSI Design

COURSE STRUCTURE (BH25 Regulations)

Applicable from AY 2025-26 Batch

I Year I Semester

S. No.	Code	Title	L	T	P	Credits
1	A5101PC	CMOS Digital IC Design	3	0	0	3
2	A5102PC	CMOS Analog IC Design	3	0	0	3
3		Professional Elective – I 1. Low Power VLSI Design (A5111PE) 2. Embedded Real Time Operating Systems (A5112PE) 3. Nanomaterials and Nanotechnology (A5113PE) 4. ARM Microcontrollers (A5114PE)	3	0	0	3
4		Professional Elective – II 1. Machine Learning and Deep Learning (A5121PE) 2. VLSI Architectures for Digital Signal Processing (A5122PE) 3. VLSI Physical Design Automation (A5123PE) 4. IoT Architectures and System Design (A5124PE)	3	0	0	3
5	A5103PC	CMOS Digital IC Design Lab	0	0	4	2
6	A5104PC	CMOS Analog IC Design Lab	0	0	4	2
7	A5105PC	Research Methodology & IPR	2	0	0	2
8		Audit Course – I	2	0	0	0
		Total Credits	16	0	8	18

I Year II Semester

S. No.	Code	Title	L	T	P	Credits
1	A5201PC	Mixed Signal IC Design	3	0	0	3
2	A5202PC	FPGA Based System Design	3	0	0	3
3		Professional Elective – III 1. VLSI Test and Testability (A5211PE) 2. Scripting Languages for Design Automation (A5212PE) 3. Functional Verification using System Verilog and UVM (A5213PE) 4. SoC Design (A5214PE)	3	0	0	3
4		Professional Elective – IV 1. Device Modelling (A5221PE) 2. Microchip Fabrication Techniques (A5222PE) 3. Power Management IC Design (A5223PE) 4. Hardware and Software Co-Design (A5224PE)	3	0	0	3
5	A5203PC	Mixed Signal IC Design Lab	0	0	4	2
6	A5204PC	FPGA Based System Design Lab	0	0	4	2
7	A5205CC	Mini Project with Seminar	0	0	4	2
8		Audit Course- II	2	0	0	0
		Total Credits	14	0	12	18

II Year I Semester

S. No.	Code	Title	L	T	P	Credits
1		Professional Elective – V 1. CMOS RF IC Design (A5311PE) 2. Hardware Security in VLSI Design (A5312PE) 3. Advanced Memory Design and Architectures (A5313PE) 4. Optimization Techniques in VLSI Design (A5314PE)	3	0	0	3
2		Open Elective	3	0	0	3
3	A5301DS	Dissertation Work Review – II	0	0	12	6
		Total Credits	6	0	12	12

*Note: For Dissertation Work Review - I, please refer 7.9 and 7.10 in Academic Regulations.

II Year II Semester

S. No.	Code	Title	L	T	P	Credits
1	A5401DS	Dissertation Work Review - III	0	0	12	06
2	A5402DS	Dissertation Viva-Voce	0	0	28	14
		Total Credits	0	0	40	20

Open Elective

Code	Title	L	T	P	Credits
A5300OE	Business Analytics	3	0	0	3
A5301OE	Entrepreneurship and Start-Ups				
A5302OE	Big Data Analytics				
A5303OE	Advanced Computer Networks				

*Open Electives may change as per JNTUH and BoS guidelines

Audit Course-I & II

Code	Title	L	T	P	Credits
A5501AC	English for Research Paper Writing	2	0	0	0
A5502AC	Disaster Management				
A5503AC	Sanskrit for Technical Knowledge				
A5504AC	Value Education				
A5505AC	Constitution of India				
A5506AC	Pedagogy Studies				
A5507AC	Stress Management by Yoga				
A5508AC	Personality Development Through Life Enlightenment Skills				

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5101PC	CMOS Digital IC Design	3	0	0	3

Course Description: This course introduces students to the foundational and advanced concepts in CMOS (Complementary Metal-Oxide-Semiconductor) digital integrated circuit design. Students will explore the principles, performance metrics, and design strategies for static and dynamic CMOS inverters, Combinational and sequential logic gates, and complex digital systems.

Course Outcomes: After completion of this course, the students will be able to

- C101.1 Understand the principles of CMOS technology and analyse the static and dynamic behavior of CMOS inverters including performance metrics such as delay, power, and energy.
- C101.2 Evaluate the impact of technology scaling on CMOS inverter characteristics and overall circuit performance.
- C101.3 Apply CMOS design techniques to implement combinational logic circuits using static, ratioed, pass-transistor, and dynamic logic styles.
- C101.4 Design and analyse sequential circuits including latches, flip-flops, and pipelined architectures with consideration of timing parameters.
- C101.5 Examine different digital IC implementation strategies including full-custom, semi-custom, and array-based design methodologies.
- C101.6 Analyse the effects of interconnect parasitics (capacitive, resistive, and inductive) and apply appropriate techniques to improve circuit performance.

Unit – I The CMOS Inverter

Introduction, the static CMOS inverter, Evaluating the robustness of the CMOS inverter – static behavior, Performance of CMOS inverter – dynamic behavior, Power, energy and energy-delay, Technology scaling and its impact on the inverter metrics.

Unit – II Designing Combinational Logic Gates in CMOS

Introduction, Static CMOS design – complementary CMOS, ratioed logic, pass-transistor logic, Dynamic CMOS design – basic principles, speed and power dissipation of dynamic logic, Issues in dynamic design, cascading dynamic gates, choosing a logic style, Designing logic for reduced supply voltage.

Unit – III Designing Sequential Logic Circuits

Introduction – timing metrics for sequential circuits, Classification of memory elements, Static latches and registers – bistability principle, multiplexer-based latches, master-slave edge-triggered register, Low-voltage static latches, static SR flip-flops, Dynamic latches and registers – transmission gate edge-triggered registers, C2MOS, TSPCR, Pipelining – latch vs. register-based pipelines, NORA-CMOS

Unit – IV Implementation Strategies for Digital ICs

Introduction, From custom to semi-custom and structured array design approaches, Custom circuit design, Cell-based design methodology, Array-based implementation approaches.

Unit – V Coping with Interconnect

Introduction, Capacitive parasitics, Resistive parasitics, Inductive parasitics, Advanced interconnect techniques.

TEXT BOOKS

1. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. “Digital Integrated Circuits: A Design Perspective”, 2nd Ed., Pearson Education, 2003.

REFERENCE BOOKS

1. Kang, Sung-Mo (Steve), and Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3rd Ed., McGraw-Hill, 2003.
2. Uyemura, John P, “Introduction to VLSI Circuits and Systems”, Wiley, 2002.
3. Weste, Neil H.E., and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective.” 4th Ed., Pearson Education, 2011.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5102PC	CMOS Analog IC Design	3	0	0	3

Course Description: Understand MOS devices and their modelling, Design and analyse CMOS sub circuits, Design and explore amplifier architectures and characterize and improve CMOS comparators.

Course Outcomes: After completion of this course, the students will be able to

- C102.1 Explain MOS device physics, characteristics, and modeling concepts for analog IC design.
- C102.2 Analyze single-stage CMOS amplifiers such as common-source, source follower, and common-gate amplifiers.
- C102.3 Analyze differential amplifier circuits including differential pairs and common-mode response.
- C102.4 Design and analyze basic and cascode current mirror circuits.
- C102.5 Explain CMOS operational amplifier architectures including one-stage and two-stage Op-Amps.
- C102.6 Evaluate analog CMOS circuits based on performance parameters such as gain, bandwidth, and power consumption.

Unit – I MOS Device Physics and Models

Introduction to analog design, MOS device physics – General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Unit – II Single Stage Amplifiers

Basic Concepts, Common-Source Stage with resistive-load and diode-connected load, Source Follower, Common-Gate Stage.

Unit – III Differential Amplifiers

Single-Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Mode with MOS Loads, Gilbert Cell.

Unit – IV Passive and Active Current Mirrors

Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

Unit – V Operational Amplifiers

General Considerations, One-Stage Op Amps, Two-Stage Op Amps, Gain Boosting, Comparison.

TEXT BOOKS

1. Razavi, Behzad, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill Education, 2001.

REFERENCE BOOKS

1. Allen, Philip E., and Douglas R. Holberg, “CMOS Analog Circuit Design”, 3rd Ed., Oxford University Press, 2011.
2. Johns, David A., and Ken Martin, “Analog Integrated Circuit Design”, Wiley India, 2015.
3. Sansen, Willy M.C., “Analog Design Essentials”, Springer, 2006.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5111PE	Low Power VLSI Design	3	0	0	3

Course Description: This course provides the details of sources of power consumption in VLSI circuits and methodologies and techniques for designing circuits to consume less power.

Course Outcomes: After completion of this course, the students will be able to

- C111.1 Analyze the low power design, methodologies and emerging technologies.
- C111.2 Investigate power dissipation types and minimization strategies.
- C111.3 Formulate strategies to optimize power consumption through supply voltage scaling.
- C111.4 Implement various methods to reduce switched capacitance and leakage power.
- C111.5 Design adiabatic logic circuits with techniques like adiabatic charging and stepwise charging
- C111.6 Propose battery-aware designs to maximize battery life by managing power dissipation.

Unit – I

Introduction: Historical Background, Why Low Power? Sources of Power Dissipation, Low Power Design Methodologies.

Latch up Problems and Its Prevention – Use of Guard Rings, Use of Trenches

Short Channel Effects – Channel Length Modulation Effect, Drain Induced Barrier Lowering, Channel Punch Through.

Emerging Technologies for Low Power – Hi-K Gate Dielectric, Lightly Doped Drain – Source, Silicon on Insulator, FinFET.

Unit – II

Sources of Power Dissipation – Short Circuit Power Dissipation, Switching Power Dissipation, Glitching Power Dissipation, Leakage Power Dissipation.

Unit – III

Supply Voltage Scaling for Low Power – Device Feature Size Scaling, Parallelism, Pipelining, Voltage Scaling using High Level Transformations, Multilevel Voltage Scaling, Dynamic Voltage and Frequency Scaling, Adaptive Voltage Scaling.

Unit – IV

Switched Capacitance Minimization – System Level Approach: Hardware Software CO-Design, Bus Encoding, Clock Gating, Glitching Power Minimization.

Leakage Power Minimization – VTCMOS Approach, Transistor Stacking, MTCMOS Approach, Power Gating.

Unit – V

Adiabatic Logic Circuits – Adiabatic Charging, Adiabatic Amplification, Adiabatic Logic Gates, Pulsed Power Supply, Stepwise Charging Circuits, Partially Adiabatic Circuits.

Battery Aware Systems – The Widening Battery Gap, Overview of Battery Technologies, Battery Characteristics, Principles of Battery Discharge, Battery Modeling, Battery Drive System Design.

TEXT BOOKS

1. Ajit Pal, “Low Power VLSI Circuits and Systems”, Springer, 2015.

REFERENCE BOOKS

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Press, 2002.
2. Kiat-Seng Yeo, Kaushik Roy, “Low-Voltage, Low-Power VLSI Subsystems”, TMH Professional Engineering.
3. Siva G. Narendran, Anatha Chandrakasan, “Leakage in Nanometer CMOS Technologies”, Springer, 2005.
4. Ming-Bo Lin, “Introduction to VLSI Systems: A Logic, Circuit and System Perspective”, CRC Press, 2011.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5112PE	Embedded Real Time Operating System	3	0	0	3

Course Description: To provide basic understanding of the features of the Embedded Real-time operating systems using case studies.

Course Outcomes: After completion of this course, the students will be able to

- C112.1 Explain various basic commands and process control of UNIX/LINUX operating systems
- C112.2 Describe basic elements of Real time operating systems and their operations
- C112.3 Examine the operations of various features in Real time operating systems
- C112.4 Analyze various building blocks and I/O sub system of Real time operating systems
- C112.5 Understand concepts of Exceptions, Interrupts and Timers.
- C112.6 Illustrate various case studies of RTOS

Unit – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

Unit – II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, tasks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

Unit – III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

Unit – IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Unit – V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS

1. Qing Li, “Real Time Concepts for Embedded Systems”, Elsevier, 2011.

REFERENCE BOOKS

1. Rajkamal, “Embedded Systems- Architecture, Programming and Design”, TMH, 2007.
2. Richard Stevens, “Advanced Programming in the UNIX Environment”, Addison Wesley Professional Computing Series.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, Addison Wesley.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5113PE	Nanomaterials and Nanotechnology	3	0	0	3

Course Description: This course explores nanomaterials and nanotechnologies, focusing on their classifications, size-dependent properties, and applications. It covers synthesis methods, carbon-based nanomaterials, MEMS technologies, and carbon nanotubes (CNTs) with their applications in electronics and materials science. The course also highlights nanoelectronics and environmental applications, emphasizing their impact on sustainability.

Course Outcomes: After completion of this course, the students will be able to

- C113.1 Describe nanomaterials and nanotechnologies, their structures, properties, synthesis methods, and applications for advanced technological solutions.
- C113.2 Classify various nanomaterials based on dimension.
- C113.3 Illustrate the properties, synthesis and applications of Low-Dimensional Nanomaterials.
- C113.4 Summarize micro- and nanolithography techniques, MEMS fabrication technologies, and emerging applications, including nano photonics.
- C113.5 Analyze the properties of Carbon Nano Tubes, their growth mechanisms, and applications.
- C113.6 Explore ferroelectric materials and applications in electronics and biological systems.

Unit – I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies, Nano dimensional Materials 0D, 1D, 2D structures, Size Effects, Fraction of Surface Atoms, Specific Surface Energy and Surface Stress, Effect on the Lattice Parameter, Phonon Density of States, the General Methods available for the Synthesis of Nanostructures, precipitative, reactive, hydrothermal/solvo thermal methods, suitability of such methods for scaling , potential Uses

Unit – II

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional, nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials, Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nanomaterials.

Unit – III

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding, Introduction to Nano Phonics.

Unit – IV

CNTs: Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's, Multi-walled nanotubes, Single-walled nanotubes, Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies, Synthesis and Applications of CNT's.

Unit – V

Ferroelectric materials, coating, molecular electronics and nanoelectronics, biological and environmental, membrane-based application, polymer-based application.

TEXT BOOKS

1. I Gusev and A A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGraw Hill Education 2012.

REFERENCE BOOKS

1. Kenneth J. Klabunde and Ryan M. Richards, “Nanoscale Materials in Chemistry”, 2nd edition, John Wiley and Sons, 2009.
2. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
3. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1st edition, 2011.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5114PE	ARM Microcontrollers	3	0	0	3

Course Description: This deals with ARM architecture, ARM RISC Philosophy, Pipelining operation, ARM instruction set and special mode of Thumb instruction mode. Also, explore ARM Cortex M3 and M4 controller, its applications, instruction set and floating-point operations in these ARM microcontrollers

Course Outcomes: After completion of this course, the students will be able to

- C114.1 Understand the ARM Processor Architectural Features
- C114.2 Write simple programs using ARM Instruction set
- C114.3 Write simple programs using ARM Instruction set in Thumb special mode
- C114.4 Differentiate between ARM Cortex M3, M4 microcontroller architectural features
- C114.5 Know the instruction set of ARM Cortex M microcontrollers.
- C114.6 Realize the floating-point operations supported in ARM Cortex M controllers.

Unit – I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model-operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

Unit – II

Introduction to the ARM Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

Unit – III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

Unit – IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

Unit – V

Floating Point Operations About Floating-Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS

1. Andrew N, Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier Publications, 2004
2. Joseph Yiu, “The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors”, Elsevier, Publications, 3rd Edition, 2014

REFERENCE BOOKS

1. Steve Furber, “ARM System on Chip Architectures”, Addison Wesley, 2nd Edition, 2000.
2. David Seal, “ARM Architecture Reference Manual”, Addison Wesley, 2nd Edition, 2000.
3. Trevor Martin, “The Designer's Guide to the Cortex-M Processor Family: A Tutorial Approach”, Elsevier Publications, 2016

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5121PE	Machine Learning and Deep Learning	3	0	0	3

Course Description: This course introduces the principles and practices of Machine Learning and Deep Learning, focusing on both theoretical understanding and practical implementation. It begins with the fundamentals of machine learning, including learning paradigms, model evaluation, and the challenges that have led to deep learning advances.

Course Outcomes: After completion of this course, the students will be able to

- C121.1 understand overfitting, underfitting, bias-variance tradeoff, and why deep learning is needed.
- C121.2 set up network structures and train them using backpropagation and activation functions.
- C121.3 apply regularization methods (like Dropout) and optimizers (like Adam).
- C121.4 use convolution and pooling layers to extract spatial features from visual data.
- C121.5 model time-series, text, and sequences while overcoming long-term memory issues.
- C121.6 pick metrics, tune hyperparameters, debug models, and apply deep learning to vision and NLP tasks.

Unit – I Machine Learning Basics

Learning algorithms, Capacity, overfitting and underfitting, estimators, bias and variance, maximum likelihood estimation, Bayesian statistics, Supervised and unsupervised learning algorithms, building a machine learning algorithm, challenges motivating deep learning.

Unit – II Deep Feedforward Networks

Gradient-based learning, hidden units, architecture design, back-propagation and other differentiation algorithms.

Unit – III Regularization for Deep Learning

Norm penalties, Dataset augmentation, multi-task learning, early stopping, sparse representations, ensemble methods, dropout.

Optimization: Optimization for Training Deep Models, challenges in neural network optimization, basic algorithms, parameter initialization strategies, algorithms with adaptive learning rates.

Unit – IV Convolutional Neural Networks

The convolution operation, motivation, pooling, convolution and pooling as an infinitely strong prior, variants of the basic convolution function, structures outputs, data types, efficient convolution algorithms, random or unsupervised features.

Sequence Modeling:

Recurrent and Recursive Nets, Recurrent Neural Networks, Recursive Neural Networks, Long Short-Term Memory, optimization for long-term dependencies.

Unit – V

Practical Methodology: Performance metrics, selecting hyperparameters, debugging strategies.

Applications: Large-scale deep learning, computer vision, speech recognition, natural language processing, other applications.

TEXT BOOKS

1. Goodfellow, Ian, Yoshua Bengio, and Aaron Courville, “Deep Learning”, MIT Press, 2016.

REFERENCE BOOKS

1. Géron, Aurélien. “Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow”, 2nd Ed., O'Reilly Media, 2019.
2. Bishop, Christopher M, “Pattern Recognition and Machine Learning”, Springer, 2006.
3. Chollet, François, “Deep Learning with Python”, 2nd Ed., Manning Publications, 2021.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5122PE	VLSI Architectures for Digital Signal Processing	3	0	0	3

Course Description: This course provides a comprehensive study of Very Large-Scale Integration (VLSI) architectures tailored for Digital Signal Processing (DSP) systems. It explores the principles, techniques, and hardware implementations that support high-performance DSP applications in modern CMOS technologies.

Course Outcomes: After completion of this course, the students will be able to

- C122.1 Explain DSP systems, data-flow graphs, iteration bound, pipelining, parallel processing, and retiming techniques.
- C122.2 Apply unfolding and folding transformations for optimized DSP architectures
- C122.3 Analyze and implement fast convolution algorithms for DSP applications.
- C122.4 Design bit-level and redundant arithmetic architectures for VLSI DSP systems
- C122.5 Explain the architecture and applications of programmable DSP processors.
- C122.6 Analyze and optimize VLSI architectures for Digital Signal Processing by applying algorithms, arithmetic architectures, and programmable DSP processor concepts.

Unit – I

Introduction to Digital Signal Processing Systems: Introduction, typical DSP algorithms, DSP application demands and scaled CMOS technologies.

Iteration Bound: Data-flow graph representations, loop bound, and iteration bound, algorithms for computing iteration bound.

Pipelining and Parallel Processing: Introduction, pipelining of FIR digital filters, parallel processing.

Retiming: Definitions and properties, solving systems of inequalities, retiming techniques.

Unit – II

Unfolding: An algorithm for unfolding, properties and applications of unfolding.

Folding: Folding transformation, register minimization techniques, folding of multirate systems

Unit – III

Fast Convolution: Introduction, Cook-Toom algorithm, Winograd algorithm, iterated convolution, cyclic convolution, design of fast convolution algorithm by inspection.

Unit – IV

Bit-Level Arithmetic Architectures: Introduction, parallel multipliers, bit-serial multipliers, bit-serial filter design and implementation.

Redundant Arithmetic: Introduction, redundant number representations, carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures, data format conversion, redundancy to nonredundant converter.

Unit – V

Programmable Digital Signal Processors: Introduction, evolution of programmable digital signal processors, important features of DSP processors, DSP processors for mobile and wireless communications, processors for multimedia signal processing.

TEXT BOOKS

1. Parhi, Keshab K, “VLSI Digital Signal Processing Systems: Design and Implementation”, Wiley, 1999.

REFERENCE BOOKS

1. V. K. Madisetti, “VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis”, IEEE Press, New York.
2. Meyer-Baese, Uwe, “Digital Signal Processing with Field Programmable Gate Arrays”, 4th Ed., Springer, 2014.
3. S. Y. Kung, H. J. Whitehouse, “VLSI and Modern Signal Processing”, Prentice Hall.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5123PE	VLSI Physical Design Automation	3	0	0	3

Course Description: To learn the concepts of VLSI physical design automation, physical design like floor planning, partitioning and placement. To learn concepts related to physical design like routing and different routing techniques and compaction algorithms.

Course Outcomes: After completion of this course, the students will be able to

- C123.1 Study automation process for VLSI System design
- C123.2 Understand fundamentals for various physical design CAD tools
- C123.3 Understand of fundamental concepts in physical design
- C123.4 Develop and enhance the algorithms and computational techniques for Physical design process of VLSI systems.
- C123.5 Understand of various Routing process and algorithms
- C123.6 Gain knowledge on the methodologies involved in chip design.

Unit – I VLSI Physical Design Automation

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

Unit – II Partitioning & Floor planning

Partitioning: Problem formulation, Design Style Specific Partitioning Problems, Classification of Partitioning Algorithms, Group Migration Algorithms- Kernighan-Lin Algorithm, Extensions of Kernighan-Lin Algorithm, Ratio Cut, Performance Driven Partitioning.

Floor planning: Design Style Specific Floor Planning Problems, Classification of Floor planning Algorithms - Constraint Based Floor planning, Rectangular Dualization.

Unit – III Pin Assignment & Placement

Pin Assignment - Problem Formulation, Design Style Specific Pin Assignment Problems, Classification of Pin Assignment Algorithms, General Pin Assignment, Channel Pin Assignment.

Placement: Problem formulation, Design Style Specific Placement Problems, Classification of Placement Algorithms, Simulation based placement algorithms, Simulated Annealing, Simulated Evolution, Partitioning based placement algorithms, Breuer's Algorithm, Terminal Propagation Algorithm, Performance driven placement.

Unit – IV Global Routing and Detailed Routing

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

Unit – V Physical Design Automation of FPGAs

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. physical design automation of MCMs. Introduction to MCM Technologies, MCM Physical Design Cycle.

TEXT BOOKS

1. Naveed Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, 2005.
2. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Wiley, 2008, 2nd Edition.

REFERENCE BOOKS

1. Sait, Sadiq M., “VLSI Physical Design Automation”, IEEE, 1995
2. Hill & Peterson, “Computer Aided Logical Design with Emphasis on VLSI”, Wiley, 1993.
3. Sadiq M Sait, Habib Youssef, “VLSI Physical Design Automation-Theory and Practice”, World Scientific.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5124PE	IoT Architectures and System Design	3	0	0	3

Course Description: A thorough introduction to the Internet of Things (IoT), covering its evolution, core technologies, practical applications, hands-on experience with Arduino and Raspberry Pi for system implementation, and exploration of challenges and emerging trends in sectors like agriculture, healthcare, and smart cities.

Course Outcomes: After completion of this course, the students will be able to

- C124.1 Gain a comprehensive understanding of the Internet of Things (IoT), application areas and enabling technologies
- C124.2 Compare M2M and IoT systems, focusing on value chains and the impact of SDN and NFV
- C124.3 Develop and implement IoT solutions on Arduino, and Raspberry Pi, using different programming languages.
- C124.4 Understand various IoT architecture components and be able to compare different IoT architectures
- C124.5 Identify and address IoT system design challenges and emerging applications in various domains.
- C124.6 Apply IoT principles to develop solutions for specific areas such as smart cities and transportation.

Unit – I IoT introduction

Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

Unit – II IoT and M2M

M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT. M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

Unit – III IoT Hands-on

Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

Unit – IV IoT Architecture

IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack.

Unit – V IoT System design

Challenges associated with IoT, Emerging pillars of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy, “Introduction to IoT”, Cambridge University Press.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry, “IoT Fundamentals Networking technologies, protocols, and use cases for IoT”, Cisco Press

REFERENCE BOOKS

1. Cuno pfister, “Getting started with the internet of things”, O Reilly Media, 2011
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications.
3. Arshdeep Bahga, Vijay Madisetti, “Internet of Things A Hands-on approach”, Universities Press.
4. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, “Internet of things”, John Wiley and Sons.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5103PC	CMOS Digital IC Design Laboratory	0	0	4	2

Course Description: This course provides a comprehensive introduction to CMOS digital circuit design, focusing on the fundamental building blocks such as inverters, combinational and sequential logic circuits, and their implementation strategies.

Course Outcomes: After completion of this course, the students will be able to

- C103.1 Design and simulate CMOS inverter and basic logic gates, and evaluate their voltage transfer characteristics, noise margins, and transient response.
- C103.2 Analyse timing performance of CMOS circuits by measuring propagation delay, rise/fall times, and the impact of load capacitance on circuit behavior.
- C103.3 Implement and compare different CMOS design styles including static, dynamic, and pass-transistor logic, and evaluate their power, delay, and output characteristics.
- C103.4 Design and verify sequential circuits and digital systems, and analyze the effects of interconnect parasitics (R, C, L) on signal integrity and overall circuit performance.

List of Experiments (Minimum 12 Experiments)

1. **Measure Voltage Transfer Characteristic (VTC) of CMOS Inverter:** Design a static CMOS inverter and plot the input vs. output voltage to determine switching threshold and noise margins.
2. **Determine Propagation Delay of CMOS Inverter:** Apply a square wave input, simulate the output waveform, and measure the rise time, fall time, and propagation delay.
3. **Design and Simulate CMOS NAND Gate:** Implement a 2-input NAND gate using CMOS and verify its truth table and transient response.
4. **Compare Static CMOS and Pass-Transistor NAND Gate:** Design both logic styles for NAND gate, simulate output voltage levels, and compare delay and power.
5. **Design a Dynamic CMOS NOR Gate:** Create a dynamic NOR gate, simulate precharge and evaluation phases, and observe output waveform timing.
6. **Implement and Simulate a Static SR Latch:** Design an SR latch using CMOS transistors; verify bistability by applying input set/reset sequences.
7. **Design a Master-Slave D Flip-Flop:** Build a master-slave edge-triggered flip-flop, apply clock and data inputs, and verify timing and output behavior.
8. **Compare Latch-Based and Register-Based Pipeline Stages:** Design a simple 2-stage pipeline using latches and registers; simulate and compare data propagation delays.
9. **Custom vs Standard Cell Design of a 2-Input AND Gate:** Implement a 2-input AND gate using full custom transistor-level design and standard cell approach; compare layout area.
10. **Array-Based Implementation of a 2-Bit Adder:** Design a 2-bit adder using an array-based logic style; simulate functional correctness and evaluate area.
11. **Analyze Delay Due to Capacitive Load on CMOS Inverter:** Add different load capacitances to inverter output and simulate the resulting delay variation.
12. **Effect of Interconnect Resistance on Signal Propagation:** Model a resistive interconnect connected to a CMOS inverter output; simulate delay and signal attenuation.
13. **Simulate Interconnect RC Parasitics Impact on Output Waveform:** Extract parasitic RC values for a simple wire segment and simulate their effect on signal rise and fall times.
14. **Compare Signal Integrity with and without Interconnect Inductance:** Model a simple interconnect with inductance; simulate signal ringing and delay effects compared to purely RC models.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5104PC	CMOS Analog IC Design Laboratory	0	0	4	2

Course Description: This laboratory course complements the theory of analog CMOS design by providing hands-on experience with MOS device characterization, amplifier circuits, differential pairs, current mirrors, and operational amplifiers.

Course Outcomes: After completion of this course, the students will be able to

- C104.1 Extract key NMOS/PMOS device parameters by analyzing SPICE-simulated I-V characteristics.
- C104.2 Design and optimize single-stage CMOS amplifiers to satisfy gain, impedance, and bandwidth specifications.
- C104.3 evaluate analog sub-circuits like current mirrors, differential pairs, and mixers for high CMRR and matching accuracy.
- C104.4 Design, simulate, and stabilize a Two-Stage CMOS Op-Amp for target gain, bandwidth, and phase margin.

List of Experiments (Minimum 12 Experiments)

1. **MOSFET I-V Characteristics Simulation:** Design and simulate NMOS and PMOS transistors to plot ID vs VDS and ID vs VGS characteristics; analyze threshold voltage and saturation behavior.
2. **Effect of Second-Order Parameters on MOS Device Performance:** Simulate and study effects like channel length modulation, body effect, and velocity saturation on transistor I-V characteristics.
3. **Extraction of MOS Device Model Parameters Using SPICE:** Extract and verify MOSFET parameters (threshold voltage, mobility, etc.) from device simulation for different model levels.
4. **Design and Simulation of Common-Source Amplifier with Resistive Load:** Design a common-source amplifier and analyze voltage gain, input/output impedance, and frequency response.
5. **Design and Simulation of Common-Source Amplifier with Diode-Connected Load:** Implement a CS amplifier with diode-connected load and compare gain and linearity with resistive-load version.
6. **Design and Analysis of Source Follower (Common-Drain) Amplifier:** Build a source follower circuit; simulate and measure voltage gain, output impedance, and linearity.
7. **Design and Simulation of Common-Gate Amplifier:** Design a common-gate stage and analyze its input/output characteristics and high-frequency response.
8. **Design of Basic Differential Pair with Resistive Load:** Simulate a differential pair and analyze differential gain, common-mode gain, and calculate CMRR.
9. **Differential Amplifier with MOS Current Mirror Load:** Implement a differential pair with active current mirror load; analyze improvements in gain and CMRR.
10. **Simulation of Gilbert Cell Mixer:** Design a Gilbert cell circuit and simulate frequency mixing operation with two sinusoidal inputs.
11. **Design and Simulation of Basic Current Mirror:** Implement a basic current mirror; simulate output current accuracy and dependence on transistor sizing.
12. **Design and Simulation of Cascode Current Mirror:** Build a cascode current mirror; analyze output impedance and current matching improvement.
13. **Design of Active Current Mirror Circuits:** Implement Wilson or improved current mirrors; simulate and compare performance with basic and cascode types.
14. **Design and Simulation of Two-Stage CMOS Operational Amplifier:** Design a two-stage op-amp; analyze gain, phase margin, unity gain bandwidth, and frequency response.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5105PC	Research Methodology and IPR	2	0	0	2

Course Description: To understand the research problem, literature studies, plagiarism, ethics, knowledge about technical writing, the nature of intellectual property rights and new developments, the patent rights.

Course Outcomes: After completion of this course, the students will be able to

- C105.1 Understand research problem formulation.
- C105.2 Analyze research related information
- C105.3 Follow research ethics
- C105.4 Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- C105.5 Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- C105.6 Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Unit – I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

Unit – II

Effective literature studies approaches, analysis, Plagiarism, Research ethics

Unit – III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

Unit – IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit – V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS

1. Melville, Stuart, and Wayne Goddard, "Research Methodology: An Introduction for Science & Engineering Students".

2. Goddard, Wayne, and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS

1. Kumar, Ranjit, "Research Methodology: A Step-by-Step Guide for Beginners", 2nd Ed
2. Halbert, Debora J, "Resisting Intellectual Property", Taylor & Francis, 2007.
3. Mayall, W. H, "Industrial Design", McGraw-Hill, 1992.
4. Niebel, Benjamin W, "Product Design", McGraw-Hill, 1974.
5. Asimov, Morris, "Introduction to Design", Prentice Hall, 1962.
6. Merges, Robert P., Peter S. Menell, and Mark A. Lemley, "Intellectual Property in the New Technological Age", 2016.
7. Ramappa, T, "Intellectual Property Rights under WTO", S. Chand, 2008

M. Tech. I Year II Semester					
Course Code	Course Title	L	T	P	Credits
A5201PC	Mixed Signal IC Design	3	0	0	3

Course Description: This course provides a solid foundation in the analysis and design of mixed-signal integrated circuits (ICs), which combine analog and digital functionality on a single chip.

Course Outcomes: After completion of this course, the students will be able to

- C201.1 Understand and analyze sinusoidal, in-phase and quadrature signals using complex plane representation.
- C201.2 Analyze sampling techniques including impulse sampling, decimation and interpolation, and evaluate aliasing effects.
- C201.3 Design and evaluate sample-and-hold (S/H) circuits and understand their spectral response and practical implementation issues.
- C201.4 Design and analyze analog filter building blocks such as active-RC, MOSFET-C and gm-C integrators.
- C201.5 Analyze digital filter structures including FIR and Sinc filters and understand ADC/DAC modeling using SPICE.
- C201.6 Evaluate data converter performance in terms of quantization noise, SNR and techniques for improving resolution and linearity.

Unit – I **Signals, Filters and Tools**

Sinusoidal signals, in-phase and quadrature signals, the complex (z-) plane, comb filters – the digital comb filter, the digital differentiator, the digital integrator, representing signals – exponential Fourier series, Fourier transform, Dirac Delta function.

Unit – II **Sampling and Aliasing**

Sampling – impulse sampling, decimation, the sample-and-hold (S/H), S/H spectral response, the reconstruction filter (RCF), circuit concerns for implementing the S/H, interpolation, Zero padding, Hold register, linear interpolation, K-path sampling – switched-capacitor circuits, non-overlapping clock generation, implementing the S/H, the S/H with gain.

Unit – III **Analog Filters**

Integrator building blocks – low pass filters, active-RC integrators, MOSFET-C integrators, gm-C (transconductance-C) integrators, discrete-time integrators, filtering topologies – the bilinear transfer function, the quadratic transfer function.

Unit – IV **Digital Filters**

SPICE models for DACs and ADCs, the ideal DAC, the ideal ADC, Sinc-shaped digital filters, band pass and high pass Sinc filters, interpolation using Sinc filters, filtering topologies – FIR filters, the bilinear transfer function, the bilinear transfer function.

Unit – V **Data Converters**

Quantization noise, signal-to-noise ratio (SNR), clock jitter, improving SNR using averaging, the one-bit ADC and DAC, passive noise-shaping, improving SNR and linearity.

TEXT BOOKS

1. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design”, Second Edition, Wiley–IEEE Press, 2008.

REFERENCE BOOKS

1. Razavi, Behzad. Design of Analog CMOS Integrated Circuits. 2nd ed., McGraw-Hill Education, 2017.
2. Johns, David A., and Ken Martin, “Analog Integrated Circuit Design”, Wiley, 1997.
3. Sansen, Willy M.C, “Analog Design Essentials”, Springer, 2006.
4. Allen, Phillip E., and Douglas R. Holberg, “CMOS Analog Circuit Design”, 2nd Ed., Oxford University Press, 2002

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5202PC	FPGA Based System Design	3	0	0	3

Course Description: This course introduces the principles and practices of FPGA-based system design, with a strong focus on digital logic implementation, system architecture, and modern design methodologies.

Course Outcomes: After completion of this course, the students will be able to

- C202.1 Understand the fundamentals of FPGA technology, architectures, and different types of FPGA devices.
- C202.2 Apply hardware description languages (Verilog/HDL) to model and implement combinational logic circuits on FPGAs.
- C202.3 Analyse and design sequential logic circuits and finite state machines with proper clocking and performance considerations.
- C202.4 Evaluate design methodologies and develop behavioural models for FPGA-based system design.
- C202.5 Design and implement system-level architectures using buses, platform FPGAs, and multi-FPGA systems.
- C202.6 Analyse power, performance, and optimization techniques in FPGA-based designs for advanced applications.

Unit – I Introduction to FPGA-Based Systems

Introduction, basic concepts, digital design and FPGAs, FPGA-based system design, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, chip I/O, circuit design of FPGA fabrics, architecture of FPGA fabrics.

Unit – II Combinational Logic Design in FPGAs

Introduction, the logic design process, hardware description languages -modeling with HDLs, Verilog, Combinational network delay, power and energy optimization, arithmetic logic, logic implementation for FPGAs, physical design for FPGAs, the logic design process revisited

Unit – III Sequential Logic and State Machines

Introduction, the sequential machine design process, sequential design styles, rules for clocking, performance analysis, power optimization

Unit – IV Design Methodologies and Behavioral Architecture

Introduction, behavioral design, design methodologies, design example

Unit – V System-Level Design and Advanced FPGA Applications

Introduction, buses, platform FPGAs, multi-FPGA systems, Novel architectures

TEXT BOOKS:

1. Wolf, Wayne. FPGA-Based System Design. Pearson Education India, 2005.

REFERENCE BOOK:

1. Maxfield, Clive, "The Design Warrior's Guide to FPGAs: Devices, Tools and Flows", Newnes, 1st ed., 2004.
2. Trimberger, Stephen M, "Field-Programmable Gate Array Technology", Springer Science & Business Media, 2012.
3. Kuon, Ian, Russell Tessier, and Jonathan Rose, "FPGA Architecture: Survey and Challenges", Now Publishers Inc., 2007.

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5211PE	VLSI Test and Testability	3	0	0	3

Course Description: This course introduces students to digital system testing techniques and fault diagnosis in VLSI circuits. It covers fault models, test generation methods for combinational and sequential circuits, and various design-for-testability (DFT) strategies

Course Outcomes: After completion of this course, the students will be able to

- C211.1 Understand the core concepts of VLSI testing, logic simulation types, and digital circuit delay models.
- C211.2 Analyze logical fault models by evaluating fault detection, fault location, and fault dominance in digital circuits.
- C211.3 Generate test patterns and implement testable architectural configurations for both combinational and sequential logic circuits.
- C211.4 Apply ad-hoc and structured Design for Testability (DFT) methods, including classical and generic scan-based designs.
- C211.5 Design Built-In Self-Test (BIST) architectures using advanced test pattern generation methods like circular BIST.
- C211.6 Evaluate embedded RAM structures and combinational circuits using precise fault diagnosis algorithms and self-checking strategies.

Unit – I Basics of Testing and Fault Modeling

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models
 - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation
 - Delay models - Gate level Event-driven simulation.

Unit – II Test Generation for Combinational and Sequential Circuits

Test generation for combinational logic circuits - Testable combinational logic circuit design
 - Test generation for sequential circuits - design of testable sequential circuits. Design For Testability

Unit – III Design for Testability

Ad-hoc design - Generic scan-based design - Classical scan-based design – System level DFT approaches.

Unit – IV Self-Test and Test Algorithms

Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

Unit – V Fault Diagnosis

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking

TEXT BOOKS

1. Abramovici, M., M. A. Breuer, and A. D. Friedman, “Digital Systems Testing and Testable Design”. 1st ed., Jaico Publishing House, 2002.
2. Bushnell, M. L., and V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Illustrated ed., Springer Science & Business Media, 2006

REFERENCE BOOKS

1. Lala, P. K, “Digital Circuit Testing and Testability”, Academic Press, 2002.
2. Crouch, A. L, “Design for Test for Digital IC’s and Embedded Core Systems”, 1st ed., Prentice Hall International, 1999

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5212PE	Scripting Languages for Design Automation	3	0	0	3

Course Description: This course introduces the use of scripting languages—PERL, TCL, and Python—in the context of Electronic Design Automation (EDA) workflows. Students will learn to write efficient automation scripts for parsing tool outputs, managing design files, and controlling EDA tools such as synthesis and simulation environments.

Course Outcomes: After completion of this course, the students will be able to

- C212.1 Understand the fundamentals of scripting languages and their role in automating EDA tool flows.
- C212.2 Develop PERL scripts using regular expressions and data structures for efficient log parsing and report generation.
- C212.3 Apply TCL scripting to interact natively with EDA tools for synthesis, timing analysis, and simulation.
- C212.4 Construct Python scripts using system modules and standard data formats for design automation and file processing.
- C212.5 Extract the features, strengths, and trade-offs of PERL, TCL, and Python to choose the right language for specific EDA tasks.
- C212.6 integrate multi-language automation flows using shell execution and intermediate data formats like CSV and JSON.

Unit – I Introduction to Scripting Languages in EDA

Introduction to scripting and automation, Scripting vs compiled languages, Using interpreters and writing first scripts in PERL, TCL, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

Unit – II PERL Scripting

Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, using files and filehandles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

Unit – III TCL Scripting

TCL syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation.

Unit – IV Python for Design Automation and Data Processing

Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, using os, sys, and subprocess modules, Writing utility scripts for automation.

Unit – V Advanced Integration and Comparison

Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

TEXT BOOKS:

1. Schwartz, Randal L., brian d foy, and Tom Phoenix, “Learning Perl”, 7th Ed., O'Reilly Media, 2016.
2. Welch, Brent B., Ken Jones, and Jeffrey Hobbs, “Practical Programming in Tcl and Tk”, 4th Ed., Prentice Hall, 2003.
3. Sweigart, Al, “Automate the Boring Stuff with Python: Practical Programming for Total Beginners”, 2nd Ed., No Starch Press, 2019.

REFERENCE BOOKS:

1. Robbins, Arnold, “Scripting the UNIX System: Using Bash, Perl, and More”, Addison-Wesley, 2003.
2. Ousterhout, John K, “Tcl and the Tk Toolkit”, 2nd Ed., Addison-Wesley Professional, 2009.
3. Python Software Foundation. Python Language Reference Manual.
<https://docs.python.org>.

M.Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5213PE	Functional Verification using System Verilog and UVM	3	0	0	3

Course Description: This course provides a comprehensive introduction to functional verification using System Verilog and the Universal Verification Methodology (UVM). Starting with foundational System Verilog language constructs and object-oriented programming, the course gradually introduces advanced verification concepts including randomization, coverage, and inter-process communication.

Course Outcomes: After completion of this course, the students will be able to

- C213.1 Explain System Verilog fundamentals and verification concepts.
- C213.2 Develop System Verilog testbenches using interfaces, OOP, assertions, and constrained randomization.
- C213.3 Apply advanced System Verilog features, inter-process communication, and functional coverage in verification.
- C213.4 Construct UVM-based verification environments using UVM components, transactions, tests, and sequences.
- C213.5 Implement Transaction-Level Modeling (TLM) communication using UVM agents, ports, and reporting mechanisms.
- C213.6 Analyze and verify digital hardware designs using System Verilog and UVM methodologies by developing reusable and scalable verification environments.

Unit – I System Verilog Fundamentals

Verification Guidelines – Introduction, verification process, basic testbench functionality, testbench components, simulation environment phases, testbench performance. Data Types – built-in data types, arrays, linked lists, creating new types and user-defined structures, constants, strings. Procedural Statements and Routines – tasks, functions, and void functions, routine arguments, returning from a routine. Local data storage, time values.

Unit – II Testbench and OOP Concepts

Connecting the Testbench and Design–separating the testbench and design, the interface construct, stimulus timing, interface driving and sampling, connecting it all together, program-module interactions, System Verilog assertions. Basic OOP – define a class, creating new objects, object deallocation, class routines, dynamic objects, copying objects, building a testbench. Randomization – Introduction, randomization in System Verilog, constraint details, solution probabilities, valid and in-line constraints, iterative and array constraints, random control, random generators, random device configuration.

Unit – III Advanced Concepts for UVM Readiness

Threads and Interprocess Communication – working with threads, interprocess communication, events, semaphores, mailboxes, building testbench with threads and IPC. Advanced OOP and Testbench Guidelines – inheritance, factory patterns, type casting and virtual methods, composition, inheritance, and alternatives, copying an object, callbacks. Functional Coverage – coverage types, strategies, anatomy of a cover group, triggering, data sampling, cross coverage.

Unit – IV UVM Infrastructure

Introduction, UVM Components, UVM Tests, UVM Transactions, UVM Sequences

Unit – V UVM Integration & TLM (Transaction-Level Modeling) Communication

UVM Agents, Using Analysis Ports in a Testbench, Put and Get Ports in Action, UVM Reporting

TEXT BOOKS:

1. Spear, Chris. “System Verilog for Verification: A Guide to Learning the Testbench Language Features”. 2nd ed., Springer, 2014.
2. Salemi, Ray. “UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology”. Mentor Graphics, 2014.

REFERENCE BOOKS:

1. Mathur, Ashok B. “Advanced Functional Verification: Concepts and Techniques”. Springer, 2021.
2. Bhasker, J., and Rakesh Chadha. “System Verilog for Verification: A Guide to Learning the Testbench Language Features”. Prentice Hall, 2007.
3. Bergeron, Janick. “System Verilog for Verification: A Guide to Learning the Testbench Language Features”. 3rd Ed., Springer, 2012.

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5214PE	SoC Design	3	0	0	3

Course Description: This course starts off with ASIC types, differences between RISC and CISC Philosophy. Detailed study of No Instruction Set Computer is done. Simulation and Synthesis process and their importance's are studied. Few low power design techniques are studied.

Course Outcomes: After completion of this course, the students will be able to

- C214.1 Explain ASIC design strategies, CISC, RISC, NISC, and ASIP architectures, and their impact on SoC design methodologies.
- C214.2 Explain NISC control-word methodology, ADLs, NISC design flow, and Generic Netlist Representation for processor modeling and synthesis.
- C214.3 Apply simulation and verification techniques for SoC datapath, control logic, and system-level modeling.
- C214.4 Analyze low-power SoC design techniques, including power gating, clock gating, voltage scaling, and dynamic frequency/voltage scaling.
- C214.5 Apply graph theory and synthesis techniques for technology-independent and technology-dependent optimization of digital systems.
- C214.6 Analyze single-core and multi-core SoCs, dark silicon challenges, power-aware HDL coding, interconnect and clock-tree issues, and fault-tolerant designs.

Unit – I ASIC

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit – II NISC

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit – III Simulation

Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit – IV Low power SoC design / Digital system

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit – V Synthesis

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails

paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Centre, 2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip", Wiley, 2011.

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5221PE	Device Modelling	3	0	0	3

Course Description: To understand advanced semiconductor devices and technologies, various models of semiconductor devices. To understand the BJT, MOSFET and other semiconductor devices from the device modeling perspective.

Course Outcomes: After completion of this course, the students will be able to

- C221.1 Analyze MOSFET structure, device physics, scaling effects, and parasitics in modern VLSI devices.
- C221.2 Model MOS capacitor characteristics and threshold voltage considering short-channel and temperature effects.
- C221.3 Apply DC, dynamic, and small-signal MOSFET models for current and capacitance analysis.
- C221.4 Evaluate MOSFET reliability issues and use SPICE device models for simulation.
- C221.5 Extract and statistically analyze device parameters accounting for process variations.
- C221.6 Apply device modeling and Simulation techniques to predict MOSFET performance in VLSI systems.

Unit – I Fundamentals of MOSFET Structure and Device Physics

Review of semiconductor physics and p–n junction, MOS transistor structure and operation, Scaling effects and parasitics, Modern VLSI device structures

Unit – II MOS Capacitor and Threshold Voltage Modeling

MOS capacitor - physics and C–V characteristics, Threshold voltage modeling: uniform and nonuniform doping, Short-channel effects: DIBL, narrow-width effect, Temperature dependence of threshold voltage

Unit – III DC and Dynamic Modeling of MOSFETs

Charge-sheet and Pao–Sah current models, Subthreshold conduction and mobility degradation, Temperature effects on current characteristics, Capacitance models: Meyer model, charge-based model, Small-signal modeling

Unit – IV Reliability Modeling and SPICE Device Models

Hot-carrier degradation and reliability concerns, Gate and substrate currents, SPICE MOSFET models: LEVEL 1, 2, 3, Parameter definitions and usage in simulation.

Unit – V Parameter Extraction and Statistical Modeling

Measurement techniques: C–V, threshold voltage, mobility, Parameter extraction using optimization techniques, Statistical modeling for process variation, Worst-case modeling in VLSI design

TEXTBOOK

- Arora, Narain, “MOSFET Modeling for VLSI Simulation: Theory and Practice”, Springer Science & Business Media, 2007.

REFERENCE BOOKS

- Tsividis, Yannis, and Colin McAndrew. “Operation and Modeling of the MOS Transistor”. 3rd ed., Oxford University Press, 2011.

2. Sze, S. M., and Kwok K. Ng. "Physics of Semiconductor Devices". 3rd ed., Wiley, 2006.
3. Trivedi, Subarna S., and Saurabh Kumar Gupta. "Semiconductor Device Modeling and Technology". PHI Learning, 2012.
4. Muller, Richard S., and Theodore I. Kamins. "Device Electronics for Integrated Circuits". 3rd ed., Wiley, 2002.

M.Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5222PE	Microchip Fabrication Techniques	3	0	0	3

Course Description: This course provides a comprehensive introduction to the principles and processes involved in semiconductor fabrication, focusing on silicon-based microchip manufacturing.

Course Outcomes: After completion of this course, the students will be able to

- C222.1 Demonstrate knowledge of semiconductor materials including chemicals, crystal growth, and wafer preparation.
- C222.2 Analyse wafer fabrication processes including contamination control, productivity, and oxidation for yield optimization.
- C222.3 Analyse lithography processes from surface preparation to final inspection for accurate patterning.
- C222.4 Assess advanced fabrication methods such as photolithography, doping, and deposition for nanoscale devices.
- C222.5 Evaluate metallization and packaging approaches to ensure reliability of integrated circuits.
- C222.6 Integrate technical and business perspectives in wafer fabrication and IC formation for industry readiness.

Unit – I Semiconductor Industry and Materials

The Semiconductor Industry, Properties of Semiconductor Materials and Chemicals, Crystal Growth and Silicon Wafer Preparation

Unit – II Wafer Fabrication and Contamination Control

Overview of Wafer Fabrication, Contamination Control, Productivity and Process Yields, Oxidation

Unit – III Lithography Processes – Patterning Steps

The Ten-Step Patterning Process — Surface Preparation to Exposure, The Ten-Step Patterning Process — Developing to Final Inspection

Unit – IV Advanced Lithography, Doping, and Deposition

Advanced Photolithography Processes, Doping, Layer Deposition

Unit – V Metallization, Device Evaluation, Business, and Packaging

Metallization, Process and Device Evaluation, The Business of Wafer Fabrication, Introduction to Devices and Integrated Circuit Formation, Introduction to Integrated Circuits, Packaging

TEXT BOOKS:

1. Van Zant, Peter. “Microchip Fabrication: A Practical Guide to Semiconductor Processing”, 6th ed., McGraw-Hill, 2014.

REFERENCE BOOKS:

1. Ghandhi, Sorab K. “VLSI Fabrication Principles: Silicon and Gallium Arsenide”. 2nd ed., Wiley, 1994.

2. Sze, Simon M., and Kwok K. Ng. "Physics of Semiconductor Devices". 3rd ed., Wiley-Interscience, 2006.
3. Streetman, Ben G., and Sanjay Banerjee. "Solid State Electronic Devices." 7th ed., Pearson, 2014.
4. Wolf, Stephen, and Richard N. Tauber. "Silicon Processing for the VLSI Era". Vol. 1, Lattice Press, 1986.

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5223PE	Power Management IC Design	3	0	0	3

Course Description: This course provides a comprehensive understanding of modern Power Management Integrated Circuits (PMICs), emphasizing the principles, design methodologies, and implementation challenges across various topologies such as linear regulators, inductive converters, and switched-capacitor converters

Course Outcomes: After completion of this course, the students will be able to

- C223.1 Analyze the role, requirements, and architectures of Power Management ICs used in modern electronic systems.
- C223.2 Design and evaluate linear voltage regulators considering efficiency, stability, PSRR, and transient performance.
- C223.3 Apply inductive DC–DC converter principles to analyze efficiency, control methods, and compensation techniques.
- C223.4 Analyze switched-capacitor and charge pump converters for efficiency, ripple reduction, and closed-loop operation.
- C223.5 Evaluate gate drivers, sensing techniques, and protection circuits in power management ICs
- C223.6 Apply PMIC design principles and simulation techniques to predict performance and reliability of power management systems.

Unit – I Fundamentals of Power Management ICs

Role and requirements of Power Management ICs (PMICs), the smartphone as a typical example, fundamental concepts - linear regulator, the inductive DC-DC converter, the Switched capacitor converters, the hybrid converter, power delivery - lateral and vertical, integrated voltage regulator (IVR), dynamic voltage and frequency scaling (DVFS).

Unit – II Linear Voltage Regulators

Fundamental circuit and control concept, drop voltage and power efficiency, frequency behavior and stability, fast transient techniques and slew-rate enhancement, PSRR, output noise, soft-start, Advanced LDO types: capacitor-less, flipped voltage follower, Digital LDOs: ADC, digital controller, limit cycle oscillations.

Unit – III Inductive DC-DC Converters

The fundamental Buck converter, voltage conversion ratio, ripple, losses and power conversion efficiency, inductor and capacitor sizing, voltage-mode and current-mode control, Loop compensation: Type I, II, III compensators, Constant on-time and hysteretic control, DCM operation and burst mode, Boost, buck-boost, and flyback converters, Multi-phase converters: ripple cancellation, phase shedding, Single inductor multiple output (SIMO) converters.

Unit – IV Switched-Capacitor (SC) and Charge Pump Converters

Basic operation of charge pumps: diode-based and transistor-based, Parasitic effects, charge sharing, and efficiency, SC converter topologies: Dickson, ladder, Fibonacci, Charge flow modeling and output resistance, Gate drive techniques, Capacitor and switch sizing, multi-phase and multi-ratio SC converters, interleaving, ripple reduction, and closed-loop control.

Unit – V Gate Drivers, Protection, and Sensing

Gate driver architectures: CMOS inverters, cascaded drivers, Bootstrap techniques and dv/dt triggering, Level shifters: resistor-based, cross-coupled, capacitive, Current sensing methods: shunt, replica, DCR, Protection circuits: OVP, thermal shutdown, UVLO, power-on-reset, Bandgap reference circuits and trimming, Zero-cross detection and current limiting.

TEXT BOOKS

1. Wicht, Bernhard. “Design of Power Management Integrated Circuits”, Wiley, 2024.

REFERENCE BOOKS

1. Erickson, Robert W., and Dragan Maksimovic. “Fundamentals of Power Electronics.” 2nd ed., Springer, 2001.
2. Basso, Christophe. “Switch-Mode Power Supplies: SPICE Simulations and Practical Designs”. McGraw-Hill Education, 2008.
3. Wu, Jinrong, and Ray Ridley. “Power Supply Design: A Practical Guide.” Springer, 2019.

M. Tech. I Year II Semester

Course Code	Course Title	L	T	P	Credits
A5224PE	Hardware and Software Co-Design	3	0	0	3

Course Description: This course covers hardware/software co-design, emphasizing the methodologies and tools for designing, verifying, and optimizing embedded systems. Students will explore modern embedded architectures, co-design models, co-synthesis algorithms, and system-level specification languages to develop complex systems efficiently.

Course Outcomes: After completion of this course, the students will be able to

- C224.1 Understand the fundamental concepts of models and algorithms of co-design.
- C224.2 Apply various prototyping and emulation techniques to develop and simulate embedded system architectures.
- C224.3 Analyze the different compilation Tools and Techniques to Embedded Processor Architectures.
- C224.4 Acquire the knowledge of firmware development process and tools during co-design.
- C224.5 Apply various prototyping and emulation techniques to develop and simulate embedded system architectures.
- C224.6 Understand different languages for systems design and their level specifications

Unit – I Co-Design Issues & Co-Synthesis Algorithms

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit – II Prototyping and Emulation & Target Architectures

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051- Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit – III Compilation Techniques and Tools for Embedded Processor Architectures

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Unit – IV Design Specification and Verification

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

Unit – V Languages for System – Level Specification & Design- I & II

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Jorgen Staunstrup, “Hardware / Software Co- Design Principles and Practice”, Wayne Wolf – Springer, 2009.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, Kluwer Academic Publishers, 2002.

REFERENCE BOOKS

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer, 2010.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5203PC	Mixed Signal IC Design Laboratory	0	0	4	2

Course Description: This course introduces the fundamental concepts of signal processing and filter design, focusing on both analog and digital domains. Students will explore signal representation, sampling theory, aliasing, and various filtering techniques including analog integrators, digital filters, and data converters.

Course Outcomes: After completion of this course, the students will be able to

- C203.1 Analyze and represent analog and digital signals in time, frequency, and z-domains
- C203.2 Design and simulate DSP blocks such as filters, differentiators, and interpolators
- C203.3 Implement and evaluate mixed-signal circuits such as S/H, SC, and integrator blocks
- C203.4 Model and analyze ADC and DAC systems for linearity and frequency response

List of Experiments (Minimum 12 Experiments)

- Sinusoidal Signals and Quadrature Components:** Generate and analyze sinusoidal signals including their in-phase and quadrature components to understand signal representation.
- Signal Representation on Complex (z-) Plane:** Plot signals on the complex z-plane and analyze their magnitude and phase characteristics.
- Digital Comb Filter Design:** Design and simulate a digital comb filter and analyze its frequency response to understand notch filtering.
- Digital Differentiator and Integrator:** Implement digital differentiator and integrator circuits and analyze their time and frequency domain responses.
- Impulse Sampling and Aliasing Analysis:** Simulate impulse sampling and study the aliasing effect in the frequency spectrum of the sampled signal.
- Sample-and-Hold (S/H) Circuit Analysis:** Design a sample-and-hold circuit and analyze its spectral response and effect on signal reconstruction.
- Interpolation Techniques:** Implement zero padding and linear interpolation methods on sampled data to improve signal resolution.
- Switched-Capacitor Sample-and-Hold Circuit:** Design a switched-capacitor sample-and-hold circuit with non-overlapping clocks and analyze its performance.
- Active-RC Low-Pass Integrator Design:** Design and simulate an active-RC low-pass integrator filter and analyze its frequency response.
- MOSFET-C and gm-C Integrator Design:** Implement MOSFET-C and gm-C integrators, compare their characteristics and frequency response.
- Discrete-Time Integrator Design:** Design and analyze discrete-time integrator circuits to understand their filtering behavior.
- Ideal DAC and ADC Modeling:** Model ideal DAC and ADC circuits, and analyze their input-output characteristics and linearity.
- Sinc-Shaped Digital Filter Design:** Design Sinc-shaped digital filters including bandpass and highpass filters and analyze their frequency response.
- FIR Filter Implementation Using Bilinear Transfer Function:** Implement FIR filters using the bilinear transfer function and analyze filter characteristics like gain and phase response.

M. Tech. I Year I Semester

Course Code	Course Title	L	T	P	Credits
A5204PC	FPGA Based System Design Laboratory	0	0	4	2

Course Description: This laboratory course focuses on practical hands-on experience with FPGA design and implementation using Hardware Description Languages (HDLs) such as Verilog or VHDL.

Course Outcomes: After completion of this course, the students will be able to

- C204.1 Apply HDL (Verilog/VHDL) to design, simulate, and verify basic combinational and sequential digital circuits using FPGA tools.
- C204.2 Design and implement arithmetic, logic, and data processing modules such as adders, multiplexers, comparators, counters, and ALUs on FPGA platforms.
- C204.3 Analyse and develop finite state machine (FSM)-based systems and real-time applications such as sequence detectors and traffic light controllers using FPGA.
- C204.4 Implement and evaluate advanced FPGA-based systems including interfacing (7-segment display, UART), timing-based designs (PWM, RTC), and signal processing applications (filters)

List of Experiments (Any 12 Experiments)

- LED Blinking Using Verilog:** Implement a basic LED blink circuit to understand FPGA programming and output pin control.
- Design and Simulation of Basic Logic Gates using Verilog HDL:** To write HDL code for basic logic gates (AND, OR, NOT, XOR), simulate their functionality, and verify the outputs using a waveform viewer.
- Implementation of 4-bit Adder/Subtractor on FPGA:** To design and implement a 4-bit adder/subtractor using Verilog, simulate and verify functionality on an FPGA development board.
- Design of a 4x1 Multiplexer and 1x4 Demultiplexer:** To write and simulate Verilog code for a 4x1 MUX and 1x4 DEMUX and validate outputs through FPGA implementation.
- Comparator Design (2-bit or 4-bit):** Design a simple digital comparator circuit that compares two binary inputs.
- Design and Implementation of a 4-bit Synchronous Counter:** To implement a 4-bit up/down synchronous counter using HDL, simulate for timing and logic correctness, and deploy it on FPGA hardware.
- Finite State Machine (FSM) Design:** Sequence Detector-To design a Moore or Mealy FSM for sequence detection, simulate the state transitions, and implement the design on an FPGA board.
- Design and Implementation of an ALU Supporting Basic Operations:** To design an Arithmetic Logic Unit that performs basic arithmetic and logic functions (ADD, SUB, AND, OR, NOT) and test it on FPGA.
- Interfacing Seven Segment Display with FPGA:** To write HDL code to drive a seven-segment display with binary or BCD inputs and implement the interface on FPGA hardware.
- Shift Register (Left/Right):** Design a shift register that shifts input bits left or right on each clock pulse.
- Implementation of Traffic Light Controller using FSM on FPGA:** To design a traffic light controller using finite state machines, simulate its time sequence, and implement it on FPGA hardware.

12. **PWM Signal Generation using FPGA:** To implement a pulse-width modulation (PWM) generator using Verilog HDL and demonstrate its use in applications like LED brightness control.
13. **Real-Time Clock Design and Display using FPGA:** To implement a real-time clock on FPGA with hour-minute-second display and use multiplexed seven-segment display for output.
14. **Serial Input with UART Receiver (Basic):** Implement a simple UART receiver to receive serial data and blink an LED.
15. **Implementing Digital Filters (FIR/IIR) on FPGA:** To implement a basic Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter in HDL and simulate its output for given inputs.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5311PE	CMOS RF IC Design	3	0	0	3

Course Description: This course describes the design and analysis of critical RF building blocks such as low-noise amplifiers (LNAs), mixers, oscillators, frequency synthesizers and power amplifiers in CMOS technology.

Course Outcomes: After completion of this course, the students will be able to

- C311.1 Analyse RF system-level parameters such as noises and non-linearity using standard performance metrics.
- C311.2 Understand LNAs and Mixers operation and noise optimization techniques.
- C311.3 Implement CMOS oscillator circuits such as LC and ring oscillators with attention to phase noise and frequency stability.
- C311.4 Apply the principles of PLLs and frequency synthesizers.
- C311.5 Understand the concepts of transreceivers architectures and performance tests.
- C311.6 Develop CMOS-based frequency generation solutions for RF systems.

Unit – I Basic Concepts in RF Design and CMOS Technology

Nonlinearity and Time Variance: Effects of Nonlinearity, Cascaded Nonlinear Stages, Intersymbol Interference, Random Processes and Noise.

Review of CMOS technology, basic MOSFET RF equivalent circuit model, advanced MOSFET RF equivalent circuit model.

Unit – II Low-Noise Amplifiers and Mixers

Low-Noise Amplifiers: General Considerations, Input Matching, Bipolar LNAs, CMOS LNAs, Downconversion Mixers: General Considerations, CMOS Mixers, Noise in Mixers.

Unit – III CMOS Oscillator Circuits

Review of general feedback principles, fixed-frequency oscillators, ring oscillator, voltage control of oscillators, oscillator phase noise and estimation.

Unit – IV Frequency Synthesizers

Introduction to the phase lock loop – definitions and basic operation, phase detection and phase-frequency detection, loop filters, PLL noise behaviour, PLL behavioral modeling. Frequency Synthesis – PLL-based synthesizers, direct digital synthesis.

Unit – V Transceiver Architectures

Transmitter Architectures: Direct-Conversion Transmitters, Two-Step Transmitters, Receiver Architectures: Heterodyne Receivers, Homodyne Receivers, Transceiver Performance Tests.

TEXT BOOKS

1. Behzad Razavi, “RF Microelectronics”, Prentice Hall, 2nd Edition, 2011.
2. Robert H. Caverly, “CMOS RFIC Design Principles”, Artech House, 2016.

REFERENCE BOOKS:

1. Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, Cambridge University Press, 2nd Edition, 2003.
2. R. Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, Wiley IEEE Press, 3rd Edition, 2010.
3. Ali M. Niknejad, “RF CMOS: Modeling and Technology for Wireless Design”, Cambridge University Press.
4. David M. Pozar, “Microwave Engineering”, Wiley, 4th Edition, 2021.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5312PE	Hardware Security in VLSI Design	3	0	0	3

Course Description: This course provides an in-depth understanding of security challenges in modern VLSI systems, particularly within SoC and PCB designs. Students will learn how to design secure hardware design using primitives like PUFs and TRNGs through a mix of theoretical foundations and hands-on experiments.

Course Outcomes: After completion of this course, the students will be able to

- C312.1 Understand the fundamentals of hardware security, trust, vulnerabilities, attacks, and countermeasures in electronic systems.
- C312.2 Analyze hardware Trojan threats, their insertion in ASIC/FPGA flows, and suitable countermeasures.
- C312.3 Identify and assess side-channel and test-based attacks and their impact on hardware security.
- C312.4 Examine physical attacks on ICs and PCBs and the associated security challenges.
- C312.5 Apply hardware security primitives such as PUFs and TRNGs for secure system design.
- C312.6 Evaluate security assets, attack models, and trust assessment techniques across pre- and post-silicon stages.

Unit – I Introduction to Hardware Security

Overview of a computing system, layers of a computing system, hardware security vs. hardware trust, attacks, vulnerabilities and countermeasures, conflict between security and test/debug, evolution of hardware security, overview of electronic hardware – nanoscale technologies, ASICs and FPGAs, printed circuit board, embedded systems, hardware-firmware-software interaction.

Unit – II Hardware Trojans

Introduction, SoC design flow, hardware trojans, hardware trojans in FPGA designs, hardware trojans taxonomy, trust benchmarks, countermeasures against hardware trojans, hardware trojan attacks. Hardware IP Piracy and Reverse Engineering: Introduction, hardware intellectual property (IP), security issues in IP-based SoC design, security issues in FPGA, reverse engineering and tampering.

Unit – III Side-Channel Attacks

Introduction, taxonomy of side-channel attacks, uncommon side-channel attacks, power analysis attacks, electromagnetic (EM) side-channel attacks, fault-injection attacks, timing attacks. Test-Oriented Attacks: Introduction, scan-based attacks, JTAG-based attacks.

Unit – IV Physical Attacks and Countermeasures & Attacks on PCB

Introduction, reverse engineering, probing attack. Security challenges, attack models, bus snooping attack.

Unit – V Hardware Security Primitives & Trust Assessment

Introduction, physical unclonable functions (PUFs), true random number generator (TRNG), design of anti-counterfeit, existing challenges and attacks. Security and Security assets and attack models, pre-silicon and post-silicon security and trust assessment.

TEXT BOOKS

1. Bhunia, Swarup, and Mark M. Tehranipoor. "Hardware Security: A Hands-on Learning Approach", 1st Edition, Academic Press, 2019.

REFERENCE BOOKS:

1. Tehranipoor, Mark, and Cliff Wang, editors, "Introduction to Hardware Security and Trust". Springer, 2012.
2. Bhunia, Swarup, and Sandip Ray, "Fundamentals of IP and SoC Security: Design, Verification, and Debug", Springer, 2017.
3. Wolf, Marilyn, "Embedded System Interfacing: Design for the Internet-of-Things (IoT)", Morgan Kaufmann, 2019.
4. Skorobogatov, Sergei, "Semi-Invasive Attacks: A New Approach to Hardware Security Analysis", Springer, 2007.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5313PE	Advanced Memory Design and Architectures	3	0	0	3

Course Description: This course provides an in-depth exploration of memory systems and architectures in modern and next-generation computer systems.

Course Outcomes: After completion of this course, the students will be able to

- C313.1 Explain the concepts of memory hierarchy, cache organization, and virtual memory used in modern computer systems.
- C313.2 Analyze cache modeling, cache design techniques, and performance improvement methods such as advanced cache architectures and prefetching mechanisms.
- C313.3 Describe the principles of on-chip networks, including routing, message transmission, router design, and non-uniform cache architectures.
- C313.4 Analyze multicore systems with respect to parallel programming challenges, memory models, data races, and transactional memory.
- C313.5 Explain the architecture, operation, and timing aspects of DRAM systems, including DDR generations, DIMMs, and memory controllers.
- C313.6 Compare and evaluate emerging memory technologies such as Flash, FeRAM, MRAM, PCM, and ReRAM for next-generation and embedded applications.

Unit – I Caches

Memory hierarchy and the notion of caches, virtual memory, modelling and designing a cache, advanced cache design, trace caches, instruction prefetching, data prefetching.

Unit – II The On-Chip Networks

Overview of an NoC, message transmission, routing, design of a router, non-uniform cache architectures, performance aspects.

Unit – III Multicore Systems

Parallel programming, issues in parallel hardware, theoretical foundations of memory models, memory models, data races, transactional memory.

Unit – IV DRAMs

DRAM cell, capacitors used in DRAM cells, array of DRAM cells, a computer system with DRAM arrays, design issues of DRAMs, DDR generations and timing, buffered DIMMs, DRAM access protocols, DRAM timing, memory controller.

Unit – V Emerging Memory Technologies

Flash memory, ferroelectric RAM (FeRAM), magneto resistive RAM (MRAM), phase change memory (PCM), resistive RAM (ReRAM), 3D and embedded memory technologies, Introduction of Memristor

TEXT BOOKS

1. Smruti R. Sarangi, “Next-Gen Computer Architecture. Till the End of Silicon. Version 3.1”, 2023.

REFERENCE BOOKS:

1. Jacob, Bruce; Ng, Spencer W.; and Wang, David T., “Memory Systems: Cache, DRAM, Dis”, Morgan Kaufmann, 2008.
2. Sharma, Ashok K., “Semiconductor Memories: Technologies, Testing and Reliability”, Wiley-IEEE Press, 1997.
3. Hennessy, John L., and Patterson, David A., “Computer Architecture: A Quantitative Approach”, 6th Edition, Morgan Kaufmann, 2019.
4. Koeth, Brent, et al., “DRAM Circuit Design: Fundamental and High-Speed Topics”, Wiley-IEEE Press, 2007.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5314PE	Optimization Techniques in VLSI Design	3	0	0	3

Course Description: This course describes various statistical modeling methodologies, analyze different estimation techniques and learn concepts of optimization algorithms.

Course Outcomes: After completion of this course, the students will be able to

- C314.1 Apply statistical modeling techniques to analyze process variations and performance uncertainties in VLSI circuits
- C314.2 Analyze timing and power characteristics of VLSI systems using statistical timing and power analysis methods.
- C314.3 Design optimized VLSI circuits using statistical optimization techniques such as gate sizing and dynamic programming.
- C314.4 Formulate and solve convex optimization problems for power–delay trade-offs in VLSI design.
- C314.5 Apply genetic algorithms to optimize VLSI design automation tasks.
- C314.6 Evaluate and integrate optimization techniques to develop efficient and reliable VLSI design solutions.

Unit – I Statistical Modeling

Modeling sources of variations, Monte Carlo techniques, Process variation Modeling- Pelgrom's model, Principle component-based modeling, Quad tree-based modeling, Performance Modeling-Response surface methodology, delay modeling, interconnect delay models.

Unit – II Timing and Power Analysis

Timing Analysis- Block-Based Timing Analysis, Path-Based Timing Analysis, Parameter-Space Techniques, Bayesian Networks.

Power Analysis- Leakage Models, High-Level Statistical Analysis, Gate-Level Statistical Analysis, dynamic power, leakage power

Unit – III Statistical Optimization Techniques

Optimization of Process Parameters, Gate Sizing, Buffer Insertion, Threshold Voltage Assignment- Sensitivity-Based Optimization and Dynamic Programming.

Unit – IV Convex optimization

Convex sets, Convex Functions, Optimization problems, Convex optimization, Linear optimization problems, Quadratic optimization problems, Geometric programming and its applications in gate sizing and power-delay trade-offs.

Unit – V Genetic Algorithm

Introduction, GA Terminology and operators, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Mapping for FPGA- Automatic test generation, comparison of genetic algorithms with conventional optimization techniques.

Case Studies.

TEXT BOOKS

1. Ashish Srivastava, Dennis Sylvester, David Blaauw, “Statistical Analysis and Optimization for VLSI: Timing and Power”, Springer, 2005.
2. Stephen Boyd, Lieven Vandenberghe, “Convex Optimization”, Cambridge University Press, 2004.

REFERENCE BOOKS:

1. M. Huth and M. Ryan, “Logic in Computer Science Modeling and Reasoning about Systems”, Cambridge University Press, 2004.
2. Bushnell and Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed, Signal Circuits”, Kluwer Academic Publishers, 2000.
3. Pinaki Mazumder, E. Mrudnick, “Genetic Algorithm for VLSI Design, Layout and Test Automation”, Prentice Hall, 1998.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5300OE	Business Analytics	3	0	0	3

Course Description: This course describes the role of business analytics within an organization and to analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization

Course Outcomes: After Completion of this course, the student will be able to

- C300OE.1 understand principles of business analytics in business decisions in organization.
- C300OE.2 Analyze data using business analytics techniques
- C300OE.3 Analyze organizational structures of business analytics
- C300OE.4 Understand data mining techniques for forecasting.
- C300OE.5 Analyze qualitative and predictive modeling.
- C300OE.6 Translate data into clear, actionable insights

Unit – I

Business Analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

Unit – II

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data Business Analytics Technology.

Unit – III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies

Unit – IV

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models

Unit – V

Decision Analysis: Formulating Decision Problems, Decision Strategies without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

TEXT BOOKS

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, “Business Analytics-Principles, Concepts, and Applications”, 1st Edition, Pearson, 2014.
2. James Evans, “Business Analytics”, 2nd Edition, Pearson Education, 2017.

REFERENCE BOOKS

1. Gert H. N. Laursen, Jesper Thorlund, “Business Analytics for Managers: Taking Business Intelligence Beyond Reporting”, 2nd Edition, Wiley Publications, 2013.
2. S. Christian Albright, Wayne L. Winston, “Business Analytics: Data Analysis & Decision Making”, 5th Edition, Cengage Publications, 2015.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5301OE	Entrepreneurship and Start-Ups	3	0	0	3

Course Description: This course describes the engineers to inculcate the skills thereof in any professional role and to consider intrapreneurship or entrepreneurship as career choices for personal and societal growth

Course Outcomes: After Completion of this course, the student will be able to

- C301OE.1 Understand the role of an entrepreneur in the economic development
- C301OE.2 Learn different Theories of entrepreneurship, the role of Family and Non-Family entrepreneurs and problem-solving skills
- C301OE.3 Analyze Marketing, Financial Plans in Entrepreneurship.
- C301OE.4 Evaluate Structural, Financial and Managerial Problems.
- C301OE.5 Apply lean methodology to startup ideas using Business Model Canvas.
- C301OE.6 Create business plans through establishing business incubators.

Unit – I

Entrepreneurship: Definition of Entrepreneur, Entrepreneurial motivation and barriers; Internal and external factors; Types of entrepreneurs, Personality and Skill Set of an Entrepreneur, Entrepreneurship as a career for engineers, scientists, and technologists.

Unit – II

Theories of Entrepreneurship: Classification of entrepreneurship. Creativity and Innovation: Creative Problems Solving, Creative Thinking, Lateral Thinking.

Family and Non-Family Entrepreneurs: Role of Professionals, Professionalism vs. family entrepreneurs, Role of Woman entrepreneur.

Unit – III

Creativity and Entrepreneurial Plan: Idea Generation, Screening and Project Identification, Creative Performance, Feasibility Analysis: Economic, Marketing, Financial and Technical; Project Planning, Evaluation, Monitoring and Control, segmentation, Targeting and positioning of Product.

Unit – IV

Operation Problems: Incubation and Take-off, Problems encountered Structural, Financial and Managerial Problems, Types of Uncertainty. Institutional support for new ventures: Supporting organizations; Incentives and facilities; Financial Institutions and Small-scale Industries, Govt. Policies for SSIs.

Unit – V

Startups' Opportunity Assessment, Business Models, Entrepreneur talk, Clinical/ Regulatory, Sector Specific Group Briefing by Advisory Committee, Pitching, Payers and Reimbursement, Pitch practice, Investors, Business Development, Opportunities in Telangana State and India –

incubators, schemes, accelerators, Role of T-hub, WE-hub.

TEXT BOOKS

1. Bridge S. et al., “Understanding Enterprise: Entrepreneurship and Small Business”, Palgrave, 2003.
2. David H Holt, “Entrepreneurship: New Venture Creation”, Prentice Hall, 1998
3. Robert D. Hisrich, Michael P. Peters, “Entrepreneurship Development, Tata McGraw Hill

REFERENCE BOOKS

1. Marc H. Meyer and Frederick G. Crane, “New Venture Creation: An Innovator’s Guide to Entrepreneurship”, 2nd Edition, Sage Publications.
2. Byers, Dorf, Nelson, “Technology Ventures: From Idea to Enterprise”.
3. Mendelson, Costolo, “Venture Deals: Be Smarter Than Your Lawyer and Venture Capitalist – Feld”.
4. Burgstone and Murphy, “Breakthrough Entrepreneurship”.
5. Alexander Osterwalder, “Business Model Generation”.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5302OE	Big Data Analytics	3	0	0	3

Course Description: The purpose of this course is to provide the students with the knowledge of Big data Analytics principles and techniques. It is also designed to give an exposure of the frontiers of Big data Analytics.

Course Outcomes: After Completion of this course, the student will be able to

- C302OE.1 To explain the foundations, definitions, and challenges of Big Data and various Analytical tools
- C302OE.2 To comprehend Hadoop Ecosystem, Map reduce, and Hbase.
- C302OE.3 To illustrate Big Data analytics and Text Analytics using tools.
- C302OE.4 To apply visualization for big data using Tableau Software.
- C302OE.5 To assess the importance of Big Data in social media and Text Mining.
- C302OE.6 To recognize the importance of Mobile Analytics and perform it using tools.

Unit – I Overview of Big Data

Getting an Overview of Big Data: What is Big Data? History of Data Management – Evolution of Big Data, Structuring Big Data, Elements of Big Data, Big Data Analytics, Careers in Big Data, Future of Big Data.

Technologies for Handling Big Data: Distributed and Parallel Computing for Big Data, Introducing, Hadoop, Cloud Computing and Big Data, In-Memory Computing Technology for Big Data.

Unit – II Hadoop Ecosystem and Hbase

Understanding Hadoop Ecosystem: Hadoop Ecosystem, Hadoop Distributed File System, MapReduce, Hadoop YARN, Hbase, Hive, Pig and Pig Latin, Sqoop, ZooKeeper, Flume, Oozie Understanding

Map Reduce Fundamentals and Hbase: The MapReduce Framework, Techniques to Optimize MapReduce Jobs, Uses of MapReduce, Role of HBase in Big Data Processing.

Unit – III Understanding Analytics and Big Data

Understanding Analytics and Big Data: Comparing Reporting and Analysis, Types of Analytics, Points to Consider during Analysis, Developing an Analytic Team,

Understanding Text Analytics Analytical Approaches and Tools to Analyze Data: Analytical Approaches, History of Analytical Tools. Introduction to Popular Analytical Tools, Comparing Various Analytical Tools, Installing R

Unit – IV Data Visualization-I

Data Visualization-I: Introducing Data Visualization, Techniques Used for Visual Data Representation, Types of Data Visualization, Applications of Data Visualization, Visualizing Big Data, Tools Used in Data Visualization, Tableau Products

Data Visualization with Tableau (Data Visualization-II): Introduction to Tableau Software,

Tableau Desktop Workspace, Data Analytics in Tableau Public, Using Visual Controls in Tableau Public

Unit – V Social Media Analytics and Text Mining

Social Media Analytics and Text Mining: Introducing social media, Introducing Key Elements of social media, Introducing Text Mining, Understanding Text Mining Process, Sentiment Analysis, Performing Social Media Analytics and Opinion Mining on Tweets

Mobile Analytics: Introducing Mobile Analytics, Introducing Mobile Analytics Tools, Performing Mobile Analytics, Challenges of Mobile Analytics

TEXT BOOKS

1. “Big data, black book”, Dream Tech Press, 2015.
2. Seema Acharya, Subhashini Chellappan, “Big Data Analytics”, Wiley 2015.
3. Simon Walkowiak, “Big Data Analytics with R”, Packt Publishing, ISBN: 9781786466457

REFERENCE BOOKS

1. Michael Minelli, Michele Chambers, “Big Data, Big Analytics: Emerging Business Intelligence and Analytic Trends for Today’s Business”, 1st Edition, Ambiga Dhiraj, Wiley CIO Series, 2013.
2. Tom White, “Hadoop: The Definitive Guide”, 3rd Edition, O Reilly Media, 2012.
3. Arvind Sathi, “Big Data Analytics: Disruptive Technologies for Changing the Game”, 1st Edition, IBM Corporation, 2012.

M.Tech. II Year I Semester

Course Code	Course Title	L	T	P	Credits
A5303OE	Advanced Computer Networks	3	0	0	3

Course Description: This course will engage in practical exercises and projects to apply knowledge, configure network components, and troubleshoot issues.

Course Outcomes: After Completion of this course, the student will be able to

- C303OE.1 Analyze the performance characteristics, advantages, and limitations of Ethernet, Token Ring, and Wireless (802.11) protocols.
- C303OE.2 Evaluate the performance and efficiency of routing and internetworking protocols.
- C303OE.3 Implement the protocols operating on the transport layer.
- C303OE.4 Apply the knowledge and skills gained to design, configure, and troubleshoot web-based systems.
- C303OE.5 Demonstrate the knowledge of wireless links, WiFi, cellular internet access, and mobility management to design and configure wireless networks.
- C303OE.6 Determine various multimedia streaming technologies and their applications.

Unit – I

Data-link protocols: Ethernet, Token Ring and Wireless (802.11). Wireless Networks and Mobile IP: Infrastructure of Wireless Networks, Wireless LAN Technologies, IEEE 802.11 Wireless Standard, Cellular Networks, Mobile IP, Wireless Mesh Networks (WMNs), Multiple access schemes Routing and Internetworking: Network–Layer Routing, Least-Cost-Path algorithms, Non-Least-Cost-Path algorithms, Intra-domain Routing Protocols, Inter-domain Routing Protocols, Congestion Control at Network Layer.

Unit – II

Transport and Application Layer Protocols: Client-Server and Peer-To-Peer Application Communication, Protocols on the transport layer, reliable communication. Routing packets through a LAN and WAN. Transport Layer, Transmission Control Protocol (TCP), User Datagram Protocol (UDP), Mobile Transport Protocols, TCP Congestion Control. Principles of Network Applications.

Unit – III

The Web and HTTP, File Transfer: FTP, Electronic Mail in the Internet, Domain Name System (DNS), P2P File Sharing, Socket Programming with TCP and UDP, building a Simple Web Server Creating simulated networks and passing packets through them using different routing techniques. Installing and using network monitoring tools.

Unit – IV

Wireless and Mobile Networks: Introduction, Wireless links and Network Characteristics - CDMA, Wifi: 802.11 Wireless LANS, Cellular internet access, Mobility management: Principles.

Unit – V

Multimedia networking: Multimedia networking applications, streaming stored video, Voice-over-IP, Protocols for real-time conversational applications.

TEXT BOOKS

1. James F. Kuros and Keith W. Ross, “Computer Networking: A Top-Down Approach”, Pearson, 6th Edition, 2012.
2. Douglas E. Comer, “Computer Networks and Internets”, 6th Edition, Pearson.

REFERENCE BOOKS

1. Jeffrey S. Beasley and Piyasat Nilkaew, “A Practical Guide to Advanced Networking”, Pearson, 3rd Edition, 2012.
2. Jeffrey S. Beasley and Piyasat Nilkaew, “Computer Networks”, Prentice Hall.
3. Srinivasan Keshav, “Mathematical Foundations of Computer Networking”, 2012.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5501AC	English for Research Paper Writing (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to Understand that how to improve your writing skills and level of readability. Learn about what to write in each section. Understand the skills needed when writing a Title Ensure the good quality of paper at very first time submission.

Course Outcomes: After Completion of this course, the student will be able to

- C501.1 Apply correct style of referencing and use punctuation appropriately
- C501.2 Demonstrate writing meaningful sentences and coherent paragraphs
- C501.3 Show conciseness, clarity and avoid redundancy in writing
- C501.4 Summarize, evaluate literature, and write methodology, results and conclusion
- C501.5 Describe how to develop title, write abstract and introduction
- C501.6 Understand that how to improve your writing skills and level of readability

Unit – I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Unit – II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

Unit – III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit – IV

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Unit – V

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

TEXT BOOKS/REFERENCE BOOKS

1. Goldbort R (2006), “Writing for Science”, Yale University Press (available on Google Books).

2. Day R (2006), “How to Write and Publish a Scientific Paper”, Cambridge University Press.
3. Highman N (1998), “Handbook of Writing for the Mathematical Sciences”, SIAM Highman’s book.
4. Adrian Wallwork, “English for Writing Research Papers”, Springer New York Dordrecht Heidelberg London, 2011.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5502AC	Disaster Management (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations. Evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

Course Outcomes: After Completion of this course, the student will be able to

- C502.1 Understand the concept of Disaster Management Cycle and Framework
- C502.2 Explain the Applications of Science and Technology for Disaster Management & Mitigation
- C502.3 Impart knowledge of causes of various disaster
- C502.4 Understand the key concepts in disaster risk reduction and humanitarian response
- C502.5 Understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries
- C502.6 Enhance awareness of Disaster Risk Management institutional processes

Unit – I Disaster Prone Areas in India

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

Unit – II Repercussions of Disasters and Hazards

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit – III Disaster Preparedness and Management

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

Unit – IV Risk Assessment Disaster Risk

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Unit – V Disaster Mitigation

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/REFERENCE BOOKS

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies”, New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.), “Disaster Mitigation Experiences and Reflections”, Prentice Hall of India, New Delhi.
3. Goel S. L., “Disaster Administration and Management Text and Case Studies”, Deep & Deep Publication Pvt. Ltd., New Delhi.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5503AC	Sanskrit for Technical Knowledge (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to knowledge in illustrious Sanskrit, the scientific language in the world. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes: After Completion of this course, the student will be able to

- C503.1 Understand the basic Sanskrit language
- C503.2 Ancient Sanskrit literature about science & technology can be understood
- C503.3 Being a logical language will help to develop logic in students
- C503.4 Understand the students to know the basic Sanskrit Grammar and Literature
- C503.5 Understand the History of Epigraphical study in India
- C503.6 Enhance the students to know the Knowledge of ontology and trends Indian Philosophy.

Unit – I

Alphabets in Sanskrit.

Unit – II

Past/Present/Future Tense, Simple Sentences.

Unit – III

Order, Introduction of roots.

Unit – IV

Technical information about Sanskrit Literature.

Unit – V

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/REFERENCE BOOKS

1. Dr. Vishwas, “Abhyaspustakam”, Samskrita-Bharti Publication, New Delhi.
2. Prathama Deeksha,Vempati Kutumb shastri, “Teach Yourself Sanskrit”, Rashtriya Sanskrit Sansthanam, New Delhi Publication.
3. Suresh Soni, “India’s Glorious Scientific Tradition”, Ocean books (P) Ltd., New Delhi.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5504AC	Value Education (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to Understand value of education and self-development. Imbibe good values in students and let the students should know about the importance of character.

Course Outcomes: After Completion of this course, the student will be able to

- C504.1 Knowledge of self-development.
- C504.2 Learn the importance of Human values Developing the overall personality.
- C504.3 Understand the importance of value-based living.
- C504.4 Emerge as responsible citizens with clear conviction to practice values and ethics in life.
- C504.5 Become value-based professionals.
- C504.6 Contribute in building a healthy nation.

Unit – I Values and self-development

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements.

Unit – II Importance of cultivation of values

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline.

Unit – III Personality and Behavior Development

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

Unit – IV Avoid fault Thinking, Free from anger

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

Unit – V Character and Competence

Character and Competence –Holy books vs Blind faith. Self-management and good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

TEXT BOOKS/REFERENCE BOOKS

1. Chakroborty S.K., “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5505AC	Constitution of India (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights.

Course Outcomes: After Completion of this course, the student will be able to

- C505.1 Understand the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics
- C505.2 Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India
- C505.3 Understand the circumstances surrounding the foundation of the Congress Socialist Party
- C505.4 Enhance the passage of the Hindu Code Bill of 1956
- C505.5 Know the importance of Constitution and Government
- C505.6 Become Good Citizens and know their fundamental rights, duties and principles.

Unit – I History of Making of the Indian Constitution

History Drafting Committee, (Composition & Working), Philosophy of the Indian Constitution: Preamble, Salient Features.

Unit – II Contours of Constitutional Rights & Duties

Fundamental Rights Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit – III Organs of Governance

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

Unit – IV Local Administration

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayati raj: Introduction, PRI: Zila Panchayat. Elected officials and their roles, CEO Zila Panchayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit – V Election Commission

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/REFERENCE BOOKS

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar, “Framing of Indian Constitution”, 1st Edition, 2015.
3. M. P. Jain, “Indian Constitution Law”, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, “Introduction to the Constitution of India”, Lexis Nexis, 2015.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5506AC	Pedagogy Studies (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to Review existing evidence on the Review topic to inform programme design and policy making undertaken by the DfID, other Agencies and researchers.

Course Outcomes: After Completion of this course, the student will be able to

- C506.1 Develop a positive attitude towards life and teaching profession
- C506.2 Analyse the classroom teaching learning and the ability to observe classroom behaviour.
- C506.3 Understand process of communication and use them in their classroom teaching and inculcate multiculturalism
- C506.4 Use of models of teaching by applying knowledge to make teaching effective
- C506.5 Use the collaborative learning into a course in a way that aligns with students learning objectives and intended outcomes
- C506.6 Develop a positive attitude towards life and teaching profession

Unit – I Introduction and Methodology

Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

Unit – II Thematic Overview

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit – III Evidence on the effectiveness of pedagogical practices

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Unit – IV Professional development

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Unit – V Research gaps and future directions

Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

TEXT BOOKS/REFERENCE BOOKS

1. Ackers J, Hardman F (2001), "Classroom interaction in Kenyan primary schools", *Compare*, 31 (2): 245-261.
2. Agrawal M (2004), "Curricular reform in schools: The importance of evaluation", *Journal of Curriculum Studies*, 36 (3): 361 -379.
3. Akyeampong K (2003), "Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1", London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013), "Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? *International Journal Educational Development*", 33 (3): 272–282.
5. Alexander RJ (2001), "Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell"
6. Chavan M (2003), "Read India: A mass scale, rapid, 'learning to read' campaign".
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

M.Tech. I Year I Semester & II Semester

Course Code	Course Title	L	T	P	Credits
A5507AC	Stress Management by Yoga (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to achieve overall Good Health of Body and Mind. To lower blood pressure and improve heart health to become non-violent and truthfulness. To increase the levels of happiness and to eliminate all types of body pains.

Course Outcomes: After Completion of this course, the student will be able to

- C507.1 Develop healthy mind in a healthy body thus improving social health also improve efficiently
- C507.2 Develop body awareness. Learn how to use their bodies in a healthy way. Perform well in sports and academics
- C507.3 balance, flexible and stamina, strengthen muscles and connective tissues enabling good posture
- C507.4 Manage stress through breathing, awareness, meditation and healthy movement
- C507.5 Build concentration, confidence and positive self-image
- C507.6 Develop healthy mind in a healthy body thus improving social health

Unit – I

Definitions of Eight parts of yoga. (Ashtanga)

Unit – II

Yam and Niyam.

Unit – III

Do's and Don't's in life.

- i) Ahinsa, satya, astheya, bramhacharya and aparigraha
- ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Unit – IV

Asan and Pranayam

Unit – V

- i) Various yog poses and their benefits for mind & body
- ii) Regularization of breathing techniques and its effects-Types of pranayama

TEXT BOOKS/REFERENCE BOOKS

1. Janardan Swami, "Yogic Asanas for Group Training-Part-I", Nagpur.
2. Swami Vivekananda, "Rajayoga or conquering the Internal Nature", Advaita Ashrama (Publication Department), Kolkata.

Course Code	Course Title	L	T	P	Credits
A5508AC	Personality Development through Life Enlightenment Skills (Audit Course-I & II)	2	0	0	0

Course Description: This course helps the students to achieve the highest goal happily, to become a person with stable mind, pleasing personality and determination.

Course Outcomes: After Completion of this course, the student will be able to

- C508.1 Understand their Personality and achieve their highest Goals of Life
- C508.2 Learn to build Positive Attitude, Self-Motivation, enhancing Self-Esteem and Emotional Intelligence
- C508.3 Analyze and Develop Time management, Team management, Work ethics, good manners and personal and professional Etiquettes
- C508.4 Lead the nation and mankind to peace prosperity and practice emotional self-regulation
- C508.5 Learn to develop coping mechanism to manage Stress through Yoga and Meditation Techniques and develop a versatile personality
- C508.6 Study of Neetishatakam will help in developing versatile personality of students

Unit – I

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

Unit – II

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (don't's)
- Verses- 71,73,75,78 (do's)

Unit – III

Approach to day-to-day work and duties: Shrimad Bhagwad Geeta

- Chapter 2-Verses 41, 47,48
- Chapter 3-Verses 13, 21, 27, 35
- Chapter 6-Verses 5,13,17, 23, 35
- Chapter 18-Verses 45, 46, 48.
-

Unit – IV

Statements of basic knowledge: Shrimad Bhagwad Geeta:

- Chapter 2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18

Unit – V

Personality of Role model. Shrimad Bhagwad Geeta:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

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